TLB - Translation Lookaside Buffers

A Comparative Study

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What is TLB?

- Table in processor containing cross-reference between virtual and real addresses of recently referenced pages
- Hardware support !
- Leads to ”faster” subset of main memory
- Associative registers - parallel search
- Frequent TLB misses can be very costly

Comparison and Current Work

- Intel 80486 CPU had 32 associative memory registers
- Pentium III processor increased to 64 entries
- AMD and Sparc processors have multilevel TLB.
- Ways of Improving performance:
  - Increasing TLB size
  - Supporting large and multiple page sizes

References

- www.tc.cornell.edu
- csdl.computer.org
- A dynamic TLB management structure to support different page sizes: *Jung-Hoon Lee,Jang-Soo Lee, and Shin-Dug Kim*

Thank You

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