Workshop on Essential Abstractions in GCC

Spim Machine Descriptions

GCC Resource Center
(www.cse.iitb.ac.in/grc)

Department of Computer Science and Engineering,
Indian Institute of Technology, Bombay

1 July 2013
Outline

• Systematic construction of machine descriptions

• Retargetting GCC to spim
  ▶ spim is mips simulator developed by James Larus
  ▶ RISC machine
  ▶ Assembly level simulator: No need of assembler, linkers, or libraries

• Level 0 of spim machine descriptions

• Level 1 of spim machine descriptions
Part 1

Systematic Construction of Machine Descriptions
In Search of Modularity in Retargetable Compilation
In Search of Modularity in Retargetable Compilation

Phases of Compilation

Source Features

Target Features

Phase 1

Phases of Compilation

Phase n

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In Search of Modularity in Retargetable Compilation

Phases of Compilation

- Phase 1
- Phase n

Source Features

- Feature 1

Target Features

- Feature m

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In Search of Modularity in Retargetable Compilation

Source Features

Feature 1

Phases of Compilation

Phase 1

Feature 1

Feature m

Target Features

Feature k

Phase n
In Search of Modularity in Retargetable Compilation

Phases of Compilation

- Level 1
- Level p

Source Features (Cumulative)

Minimal Target Features (Cumulative)
Systematic Development of Machine Descriptions

Conditional control transfers

Function Calls

Arithmetic Expressions

Sequence of Simple Assignments involving integers

MD Level 1

MD Level 2

MD Level 3

MD Level 4

Essential Abstractions in GCC

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Systematic Development of Machine Descriptions

- Define different levels of source language
- Identify the minimal information required in the machine description to support each level
  - Successful compilation of any program, and
  - Correct execution of the generated assembly program.
- Interesting observations
  - It is the increment in the source language which results in understandable increments in machine descriptions rather than the increment in the target architecture.
  - If the levels are identified properly, the increments in machine descriptions are monotonic.
Part 2

Retargeting GCC to Spim: A Recap
Retargeting GCC to Spim

- Registering spim target with GCC build process
- Making machine description files available
- Building the compiler
We want to add multiple descriptions:

- Step 1. In the file $(SOURCE_D)/config.sub

  Add to the case $basic_machine

  - spim* in the part following
    # Recognize the basic CPU types without company name.
  - spim*-- in the part following
    # Recognize the basic CPU types with company name.
Registering Spim with GCC Build Process

- Step 2a. In the file $(SOURCE_D)/gcc/config.gcc

In case ${target} used for defining cpu_type, i.e. after the line

```
# Set default cpu_type, tm_file, tm_p_file and xm_file ...
```

add the following case

```
spim*--*--*)
    cpu_type=spim
```

This says that the machine description files are available in the directory

$(SOURCE_D)/gcc/config/spim.
Registering Spim with GCC Build Process

- Step 2b. In the file $(SOURCE_D)/gcc/config.gcc

In the case ${target}, after the case for score-*-elf), add the following

```bash
spim*-*-*)
    gas=no
    gnu_ld=no
    file_base="'echo ${target} | sed 's/-.*$//''"
    tm_file="${cpu_type}/${file_base}.h"
    md_file="${cpu_type}/${file_base}.md"
    out_file="${cpu_type}/${file_base}.md"
    tm_p_file="${cpu_type}/${file_base}-protos.h"
    echo ${target}
    ;
```
Registering Spim with GCC Build Process

- Step 2c.
  - Create the directory file $(SOURCE_D)/gcc/common/config/spim
  - Copy $SOURCE_D/gcc/common/config/default-common.c to $SOURCE_D/gcc/common/config/spim/spim-common.c
Building a Cross-Compiler for Spim

- Normal cross compiler build process attempts to use the generated cc1 to compile the emulation libraries (LIBGCC) into executables using the assembler, linker, and archiver.
- We are interested in only the cc1 compiler.
  
  Add a new target in the Makefile.in

```bash
.PHONY: cc1
cc1:
    make all-gcc TARGET-gcc=cc1$(exeext)
```
Building a Cross-Compiler for Spim

- Create directories `$\text{BUILD}_D$` and in a tree not rooted at `$\text{SOURCE}_D$`.
- Change the directory to `$\text{BUILD}_D$` and execute the commands
  
  ```
  $ \text{cd} \ \text{BUILD}_D$
  $ \text{${SOURCE}_D$}/configure \ --\text{target=spim}<n$
  $ \text{make cc1}$
  ``
- Pray for 10 minutes :-(
Part 3

Level 0 of Spim Machine Descriptions
Sub-levels of Level 0

Three sub-levels

- Level 0.0: Merely build GCC for spim simulator
  Does not compile any program (i.e. compilation aborts)

- Level 0.1: Compiles empty void functions

```c
void fun(int p1, int p2)
{
    int v1, v2;
}
```

- Level 0.2: Incorporates complete activation record structure
  Required for Level 1

```c
void fun()
{
    L: goto L;
}
```
Category of Macros in Level 0

<table>
<thead>
<tr>
<th>Category</th>
<th>Level 0.0</th>
<th>Level 0.1</th>
<th>Level 0.2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memory Layout</td>
<td>complete</td>
<td>complete</td>
<td>complete</td>
</tr>
<tr>
<td>Registers</td>
<td>partial</td>
<td>partial</td>
<td>complete</td>
</tr>
<tr>
<td>Addressing Modes</td>
<td>none</td>
<td>partial</td>
<td>partial</td>
</tr>
<tr>
<td>Activation Record Conventions</td>
<td>dummy</td>
<td>dummy</td>
<td>complete</td>
</tr>
<tr>
<td>Calling Conventions</td>
<td>dummy</td>
<td>dummy</td>
<td>partial</td>
</tr>
<tr>
<td>Assembly Output Format</td>
<td>dummy</td>
<td>partial</td>
<td>partial</td>
</tr>
</tbody>
</table>

- Complete specification of activation record in level 0.2 is not necessary but is provided to facilitate local variables in level 1.
- Complete specification of registers in level 0.2 follows the complete specification of activation record.
Memory Layout Related Macros for Level 0

#define BITS_BIG_ENDIAN 0
#define BYTES_BIG_ENDIAN 0
#define WORDS_BIG_ENDIAN 0
#define UNITS_PER_WORD 4
#define PARM_BOUNDARY 32
#define STACK_BOUNDARY 64
#define FUNCTION_BOUNDARY 32
#define BIGGEST_ALIGNMENT 64
#define STRICT_ALIGNMENT 0
#define MOVE_MAX 4
#define Pmode SImode
#define FUNCTION_MODE SImode
#define SLOW_BYTE_ACCESS 0
#define CASE_VECTOR_MODE SImode
Register Categories for Spim

All Registers

Available to Compiler

General

Floating Point

Fixed

GPRs (address + data)

Address

Data

Caller-saved

Callee-saved

Not Available to Compiler

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## Registers in Spim

<table>
<thead>
<tr>
<th>Register</th>
<th>Type</th>
<th>Size</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>$zero</code></td>
<td>constant data</td>
<td>32</td>
<td>caller</td>
</tr>
<tr>
<td><code>$at</code></td>
<td>NA</td>
<td>32</td>
<td>caller</td>
</tr>
<tr>
<td><code>$v0</code></td>
<td>result</td>
<td>32,64</td>
<td>caller</td>
</tr>
<tr>
<td><code>$v1</code></td>
<td>result</td>
<td>32</td>
<td>caller</td>
</tr>
<tr>
<td><code>$a0</code></td>
<td>argument</td>
<td>32,64</td>
<td>caller</td>
</tr>
<tr>
<td><code>$a1</code></td>
<td>argument</td>
<td>32</td>
<td>caller</td>
</tr>
<tr>
<td><code>$a2</code></td>
<td>argument</td>
<td>32,64</td>
<td>caller</td>
</tr>
<tr>
<td><code>$a3</code></td>
<td>argument</td>
<td>32</td>
<td>caller</td>
</tr>
<tr>
<td><code>$t0</code></td>
<td>temporary</td>
<td>32,64</td>
<td>caller</td>
</tr>
<tr>
<td><code>$t1</code></td>
<td>temporary</td>
<td>32</td>
<td>caller</td>
</tr>
<tr>
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<td>temporary</td>
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<td>caller</td>
</tr>
<tr>
<td><code>$t3</code></td>
<td>temporary</td>
<td>32</td>
<td>caller</td>
</tr>
<tr>
<td><code>$t4</code></td>
<td>temporary</td>
<td>32,64</td>
<td>caller</td>
</tr>
<tr>
<td><code>$t5</code></td>
<td>temporary</td>
<td>32</td>
<td>caller</td>
</tr>
<tr>
<td><code>$t6</code></td>
<td>temporary</td>
<td>32,64</td>
<td>caller</td>
</tr>
<tr>
<td><code>$t7</code></td>
<td>temporary</td>
<td>32</td>
<td>caller</td>
</tr>
</tbody>
</table>

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</thead>
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<tr>
<td><code>$s0</code></td>
<td>temporary</td>
<td>32,64</td>
<td>callee</td>
</tr>
<tr>
<td><code>$s1</code></td>
<td>temporary</td>
<td>32</td>
<td>callee</td>
</tr>
<tr>
<td><code>$s2</code></td>
<td>result</td>
<td>32,64</td>
<td>callee</td>
</tr>
<tr>
<td><code>$s3</code></td>
<td>result</td>
<td>32</td>
<td>callee</td>
</tr>
<tr>
<td><code>$s4</code></td>
<td>temporary</td>
<td>32,64</td>
<td>callee</td>
</tr>
<tr>
<td><code>$s5</code></td>
<td>temporary</td>
<td>32</td>
<td>callee</td>
</tr>
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<td><code>$s6</code></td>
<td>temporary</td>
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<td>callee</td>
</tr>
<tr>
<td><code>$s7</code></td>
<td>temporary</td>
<td>32</td>
<td>callee</td>
</tr>
<tr>
<td><code>$t8</code></td>
<td>temporary</td>
<td>32,64</td>
<td>caller</td>
</tr>
<tr>
<td><code>$t9</code></td>
<td>temporary</td>
<td>32</td>
<td>caller</td>
</tr>
<tr>
<td><code>$k0</code></td>
<td>NA</td>
<td>32,64</td>
<td>NA</td>
</tr>
<tr>
<td><code>$k1</code></td>
<td>NA</td>
<td>32</td>
<td>NA</td>
</tr>
<tr>
<td><code>$gp</code></td>
<td>global pointer</td>
<td>32,64</td>
<td>address</td>
</tr>
<tr>
<td><code>$sp</code></td>
<td>stack pointer</td>
<td>32</td>
<td>address</td>
</tr>
<tr>
<td><code>$fp</code></td>
<td>frame pointer</td>
<td>32,64</td>
<td>address</td>
</tr>
<tr>
<td><code>$ra</code></td>
<td>return address</td>
<td>32</td>
<td>address</td>
</tr>
</tbody>
</table>
Register Information in Level 0.2

```c
#define FIRST_PSEUDO_REGISTER 32

#define FIXEDRegisters
    // not for global
    /* register allocation */
    { 1, 1, 0, 0, 0, 0, 0, 0, 
      0, 0, 0, 0, 0, 0, 0, 0, 
      0, 0, 0, 0, 0, 0, 0, 0, 
      0, 0, 1, 1, 1, 1, 1, 1 }

#define CALL_USED_REGISTERS
    /* Caller-saved registers */
    { 1, 1, 1, 1, 1, 1, 1, 1, 
      1, 1, 1, 1, 1, 1, 1, 1, 
      0, 0, 0, 0, 0, 0, 0, 0, 
      1, 1, 1, 1, 1, 1, 1, 1 }

#define HARD_REGNO (R, M)
    (GET_MODE_SIZE (M) + 
     UNITS_PER_WORD - 1) / 
     UNITS_PER_WORD)

#define HARD_REGNO_OK(R,M)
    hard_regno_mode_ok (R, M)

#define MODES_TIEABLE_P(M1,M2)
    modes_tieable_p (M1,M2)

$zero,$at
$k0,$k1
$gp,$sp,$fp,$ra
$s0 to $s7
```
Register Classes in Level 0.2

```c
enum reg_class {
    NO_REGS, CALLER_SAVED_REGS, CALLEE_SAVED_REGS, BASE_REGS,
    GENERAL_REGS, ALL_REGS,
    LIM_REG_CLASSES
};

#define N_REG_CLASSES        LIM_REG_CLASSES
#define REG_CLASS_NAMES {
    "NO_REGS", "CALLER_SAVED_REGS", "CALLEE_SAVED_REGS", "BASE_REGS", "GEN_REGS", "ALL_REGS"
}

#define REG_CLASS_CONTENTS
/* Register numbers */
{
    0x00000000, 0xffff0000, 0x00ff0000, 0xf0000000, 0xc0000000, 0xffffffff
}

#define CLASS_MAX_NREGS(C, M) ((GET_MODE_SIZE (M) + UNITS_PER_WORD - 1) / UNITS_PER_WORD)

#define REGNO_OK_FOR_BASE_P(R) 1
#define REGNO_OK_FOR_INDEX_P(R) 0
#define PREFERRED_RELOAD_CLASS(X, C)
/* Max reg required for a class */
```

address registers

```c
#define REGNO_REG_CLASS(REGNO) regno_reg_class(REGNO)
#define BASE_REG_CLASS
#define INDEX_REG_CLASS NO_REGS
#define REG_CLASS_FROM_LETTER(c)
#define REGNO_OK_FOR_BASE_P(R) 1
#define REGNO_OK_FOR_INDEX_P(R) 0
#define PREFERRED_RELOAD_CLASS(X, C)
/* Max reg required for a class */
```
function calling conventions

pass arguments on stack. return values goes in register $v0 (in level 1).

#define RETURN_POPS_ARGS(FUN, TYPE, SIZE) 0
#define TARGET_FUNCTION_ARG spim_function_arg
#define FUNCTION_ARG_REGNO_P(r) 0

/*Data structure to record the information about args passed in *registers. Irrelevant in this level so a simple int will do. */
#define CUMULATIVE_ARGS int
#define INIT_CUMULATIVE_ARGS(CUM, FNTYPE, LIBNAME, FNDECL, NAMED_ARGS) \
    { CUM = 0; }
#define TARGET_FUNCTION_ARG_ADVANCE spim_function_arg_advance
#define FUNCTION_VALUE(valtype, func) function_value()
#define FUNCTION_VALUE_REGNO_P(REGN) ((REGN) == 2)
Activation Record Structure in Spim

Caller’s Activation Record
Activation Record Structure in Spim

Caller’s Responsibility

Caller’s Activation Record

Parameter $n$
Activation Record Structure in Spim

Caller’s Activation Record

Parameter $n$

Parameter $n - 1$
Activation Record Structure in Spim

Caller’s Responsibility

Caller’s Activation Record

Parameter $n$

Parameter $n - 1$

...
Activation Record Structure in Spim

Caller's Responsibility

Caller's Activation Record

Parameter $n$

Parameter $n - 1$

\ldots

Parameter 1

Argument Pointer
Activation Record Structure in Spim

Caller’s Activation Record

Parameter $n$

Parameter $n - 1$

... 

Parameter 1

Return Address

Caller’s Responsibility

Callee’s Responsibility

Argument Pointer
Activation Record Structure in Spim

- **Caller’s Activation Record**
  - Parameter $n$
  - Parameter $n - 1$
  - ... 
  - Parameter 1
  - Return Address
  - Caller’s FPR (Control Link)

- **Caller’s Responsibility**

- **Callee’s Responsibility**

- **Argument Pointer**
Activation Record Structure in Spim

Caller's Responsibility

Callee's Responsibility

Caller's Activation Record

Parameter $n$

Parameter $n-1$

...  

Parameter 1

Return Address

Caller's FPR (Control Link)

Caller's SPR

Argument Pointer
Activation Record Structure in Spim

<table>
<thead>
<tr>
<th>Caller’s Activation Record</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parameter $n$</td>
</tr>
<tr>
<td>Parameter $n-1$</td>
</tr>
<tr>
<td>...</td>
</tr>
<tr>
<td>Parameter 1</td>
</tr>
<tr>
<td>Return Address</td>
</tr>
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<td>Caller’s FPR (Control Link)</td>
</tr>
<tr>
<td>Caller’s SPR</td>
</tr>
<tr>
<td>Callee Saved Registers</td>
</tr>
</tbody>
</table>

Caller’s Responsibility

- Parameter
- Return Address
- Caller’s FPR (Control Link)
- Caller’s SPR
- Callee Saved Registers

Callee’s Responsibility

- Argument Pointer

Size is known only after register allocation
Activation Record Structure in Spim

**Caller's Activation Record**
- Parameter \( n \)
- Parameter \( n - 1 \)
- ... 
- Parameter 1
- Return Address
- Caller's FPR (Control Link)
- Caller's SPR
- Callee Saved Registers
- Local Variable 1

**Caller's Responsibility**
- Parameter \( n \)
- Parameter \( n - 1 \)
- ... 
- Parameter 1
- Return Address
- Caller's FPR (Control Link)
- Caller's SPR
- Callee Saved Registers
- Local Variable 1

**Callee's Responsibility**
- Argument Pointer
- Size is known only after register allocation
- Initial Frame Pointer
Activation Record Structure in Spim

**Caller’s Activation Record**

- Parameter $n$
- Parameter $n - 1$
- ...  
- Parameter 1

**Caller’s Responsibility**

- Return Address
- Caller’s FPR (Control Link)
- Caller’s SPR
- Callee Saved Registers
- Local Variable 1
- Local Variable 2

**Callee’s Responsibility**

- Argument Pointer

Size is known only after register allocation

Initial Frame Pointer
Activation Record Structure in Spim

Caller’s Activation Record

- Parameter $n$
- Parameter $n - 1$
- \ldots
- Parameter 1
- Return Address
- Caller’s FPR (Control Link)
- Caller’s SPR
- Callee Saved Registers
- Local Variable 1
- Local Variable 2
- \ldots

Callee’s Responsibility

Caller’s Responsibility

Size is known only after register allocation

Argument Pointer

Initial Frame Pointer
Activation Record Structure in Spim

Caller’s Activation Record

- Parameter $n$
- Parameter $n - 1$
- ... 
- Parameter 1
- Return Address
- Caller’s FPR (Control Link)
- Caller’s SPR
- Callee Saved Registers
  - Local Variable 1
  - Local Variable 2
  - ... 
  - Local Variable $n$

Callee’s Responsibility

- Initial Frame Pointer
- Stack Pointer
- Argument Pointer

Size is known only after register allocation

Essential Abstractions in GCC  
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Minimizing Registers for Accessing Activation Records

Reduce four pointer registers (stack, frame, args, and hard frame) to fewer registers.

#define ELIMINABLE_REGS
{{FRAME_POINTER_REGNUM, STACK_POINTER_REGNUM},
 {FRAME_POINTER_REGNUM, HARD_FRAME_POINTER_REGNUM},
 {ARG_POINTER_REGNUM, STACK_POINTER_REGNUM},
 {HARD_FRAME_POINTER_REGNUM, STACK_POINTER_REGNUM}
}

/Recomputes new offsets, after eliminating./

#define INITIAL_ELIMINATION_OFFSET (FROM, TO, VAR)
(VAR) = initial_elimination_offset(FROM, TO)
Specifying Activation Record

#define STARTING_FRAME_OFFSET starting_frame_offset ()
#define FIRST_PARM_OFFSET(FUN) 0
#define STACK_POINTER_REGNUM 29
#define FRAME_POINTER_REGNUM 1
#define HARD_FRAME_POINTER_REGNUM 30
#define ARG_POINTER_REGNUM HARD_FRAME_POINTER_REGNUM
Level 0.0 Machine Description File
Level 0.0 Machine Description File

Empty :-)

Essential Abstractions in GCC

GCC Resource Center, IIT Bombay
# Operations in Level 0

<table>
<thead>
<tr>
<th>Operations</th>
<th>Level 0.0</th>
<th>Level 0.1</th>
<th>Level 0.2</th>
</tr>
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<tbody>
<tr>
<td>JUMP direct</td>
<td>dummy</td>
<td>actual</td>
<td>actual</td>
</tr>
<tr>
<td>JUMP indirect</td>
<td>dummy</td>
<td>dummy</td>
<td>dummy</td>
</tr>
<tr>
<td>NOP</td>
<td>dummy</td>
<td>actual</td>
<td>actual</td>
</tr>
<tr>
<td>MOV</td>
<td>not required</td>
<td>partial</td>
<td>partial</td>
</tr>
<tr>
<td>RETURN</td>
<td>not required</td>
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## Operations in Level 0

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<tr>
<td>RETURN</td>
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</table>

---

```scheme
(define_insn "jump"
  [(set (pc)
    (label_ref (match_operand 0 "" ""))
  )]
  ""
  "j %10"
)
```
## Operations in Level 0

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### spim0.0.c
```c
rtx gen_jump (...) {
  return 0;
}
rtx gen_indirect_jump (...) {
  return 0;
}
rtx gen_nop () {
  return 0;
}
```

### spim0.0.h
```c
#define CODE_FOR_indirect_jump 8
```

### spim0.2.md
```md
(define_insn "jump"
  [(set (pc)
      (label_ref (match_operand 0 "" "")
        ""
      "j %10")
    )]
```

**Essential Abstractions in GCC GCC Resource Center, IIT Bombay**
## Operations in Level 0

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<td>actual</td>
<td>actual</td>
</tr>
<tr>
<td>JUMP indirect</td>
<td>dummy</td>
<td>dummy</td>
<td>dummy</td>
</tr>
<tr>
<td>NOP</td>
<td>dummy</td>
<td>actual</td>
<td>actual</td>
</tr>
<tr>
<td>MOV</td>
<td>not required</td>
<td>partial</td>
<td>partial</td>
</tr>
<tr>
<td>RETURN</td>
<td>not required</td>
<td>partial</td>
<td>partial</td>
</tr>
</tbody>
</table>

Only define expand. No define insn.

```
(define_expand "movsi"
   
   [(set (match_operand:SI 0 "nonimmediate_operand" ""))
    (match_operand:SI 1 "general_operand" ""))
  

  ""

  {
    if(GET_CODE(operands[0])==MEM && GET_CODE(operands[1])!=REG)
    {
      if(can_create_pseudo_p())
      {
        operands[1]=force_reg(SImode,operands[1]);
      }
    }
  }
```

spim0.2.md
# Operations in Level 0

<table>
<thead>
<tr>
<th>Operations</th>
<th>Level 0.0</th>
<th>Level 0.1</th>
<th>Level 0.2</th>
</tr>
</thead>
<tbody>
<tr>
<td>JUMP direct</td>
<td>dummy</td>
<td>actual</td>
<td>actual</td>
</tr>
<tr>
<td>JUMP indirect</td>
<td>dummy</td>
<td>dummy</td>
<td>dummy</td>
</tr>
<tr>
<td>NOP</td>
<td>dummy</td>
<td>actual</td>
<td>actual</td>
</tr>
<tr>
<td>MOV</td>
<td>not required</td>
<td>partial</td>
<td>partial</td>
</tr>
<tr>
<td>RETURN</td>
<td>not required</td>
<td>partial</td>
<td>partial</td>
</tr>
</tbody>
</table>

### Snippet from spim0.2.md

```plaintext
(define_expand "epilogue"
  [(clobber (const int 0))]
  ""
  { spim_epilogue();
    DONE;
  }
)
```

### Snippet from spim0.2.c

```c
void spim_epilogue()
{
    emit_insn(gen_IITB_return());
}
```

*Only return. No epilogue code.*
### Operations in Level 0

<table>
<thead>
<tr>
<th>Operations</th>
<th>Level 0.0</th>
<th>Level 0.1</th>
<th>Level 0.2</th>
</tr>
</thead>
<tbody>
<tr>
<td>JUMP direct</td>
<td>dummy</td>
<td>actual</td>
<td>actual</td>
</tr>
<tr>
<td>JUMP indirect</td>
<td>dummy</td>
<td>dummy</td>
<td>dummy</td>
</tr>
<tr>
<td>NOP</td>
<td>dummy</td>
<td>partial</td>
<td>partial</td>
</tr>
<tr>
<td>MOV</td>
<td>not required</td>
<td>partial</td>
<td>partial</td>
</tr>
<tr>
<td>RETURN</td>
<td>not required</td>
<td>partial</td>
<td>partial</td>
</tr>
</tbody>
</table>

(define_insn "nop"
  [(const_int 0)]
  ""
  "nop"
  )
Part 4

Level 1 of Spim Machine Descriptions
Increments for Level 1

- Addition to the source language
  - Assignment statements involving integer constant, integer local or global variables.
  - Returning values. (No calls, though!)

- Changes in machine descriptions
  - Minor changes in macros required for level 0
    - $zero now belongs to new class
    - Assembly output needs to change
  - Some function bodies expanded
  - New operations included in the .md file

`diff -w` shows the changes!
## Operations Required in Level 1

<table>
<thead>
<tr>
<th>Operation</th>
<th>Primitive Variants</th>
<th>Implementation</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dest $\leftarrow$ Src</td>
<td>$R_i \leftarrow R_j$</td>
<td>move $rj$, $ri$</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$R \leftarrow M_{global}$</td>
<td>lw $r$, $m$</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$R \leftarrow M_{local}$</td>
<td>lw $r$, $c($fp$)$</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$R \leftarrow C$</td>
<td>li $r$, $c$</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$M \leftarrow R$</td>
<td>sw $r$, $m$</td>
<td></td>
</tr>
<tr>
<td>RETURN Src</td>
<td>RETURN Src</td>
<td>$v0 \leftarrow Src$</td>
<td>level 0</td>
</tr>
<tr>
<td></td>
<td>j $ra$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dest $\leftarrow$ $Src_1 + Src_2$</td>
<td>$R_i \leftarrow R_j + R_k$</td>
<td>add $ri$, $rj$, $rk$</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$R_i \leftarrow R_j + C$</td>
<td>addi $ri$, $rj$, $c$</td>
<td></td>
</tr>
</tbody>
</table>
Move Operations in spim1.md

- Multiple primitive variants require us to map a single operation in IR to multiple RTL patterns
  \[ \Rightarrow {\text{use define\_expand}} \]
- Ensure that the second operand is in a register

```
(define_expand "movsi"
  [(set (match_operand:SI 0 "nonimmediate\_operand" ">
               (match_operand:SI 1 "general\_operand" ">
  )]
  ""
  { if(GET\_CODE(operands[0])==MEM &&
    GET\_CODE(operands[1])!=REG &&
    (can\_create\_pseudo\_p()) /* force conversion only */
    /* before register allocation */
    { operands[1]=force\_reg(SImode,operands[1]); } }
  }
)```

Essential Abstractions in GCC GCC Resource Center, IIT Bombay
Move Operations in spim1 Compiler for Assignment $a = b$

```c
(define_expand "movsi"
   [(set (match_operand:SI 0 "nonimmediate_operand" """)
       (match_operand:SI 1 "general_operand" ""))
   ""
   { if(GET_CODE(operands[0]) == MEM &&
       GET_CODE(operands[1]) != REG &&
       (can_create_pseudo_p()) /* force conversion only */
       /* before register allocation */
       { operands[1] = force_reg(SImode, operands[1]); } }
)}

(insn 6 5 7 3 t.c:25 (set (reg:SI 38)
      (mem/c/i:SI (plus:SI (reg/f:SI 33 virtual-stack-vars)
      (const_int -4 [0xffffffffc]) [0 b+0 S4 A32])) -1 (nil))
(insn 7 6 8 3 t.c:25 (set (mem/c/i:SI (plus:SI (reg/f:SI 33 virtual-stack-vars)
      (const_int -8 [0xffffffff8]) [0 a+0 S4 A32])
      (reg:SI 38)) -1 (nil))
```
Move Operations in spim1 Compiler for Assignment $a = b$

```
(define_expand "movsi"
  [(set (match_operand:SI 0 "nonimmediate_operand" "")
      (match_operand:SI 1 "general_operand" "")
    ]
  ""
  
  { if(GET_CODE(operands[0])==MEM &&
      GET_CODE(operands[1])!=REG &&
      (can_create_pseudo_p()) /* force conversion only */
      /* before register allocation */
      { operands[1]=force_reg(SImode,operands[1]); } } )

(insn 6 5 7 3 t.c:25 (set (reg:SI 38)
    (mem/c/i:SI (plus:SI (reg/f:SI 33 virtual-stack-vars)
      (const_int -4 [0xffffffffc])) [0 b+0 S4 A32])) -1 (nil))

(insn 7 6 8 3 t.c:25 (set (mem/c/i:SI (plus:SI (reg/f:SI 33 virtual-
    (const_int -8 [0xffffffff8])) [0 a+0 S4 A32])
    (reg:SI 38)) -1 (nil))
```
**Move Operations in spim1.md**

- **Load from Memory** \( R \leftarrow M \)

  \[
  \text{(define_insn "*load_word"}
  \[
  \begin{align*}
  &\text{[(set (match_operand:SI 0 "register_operand" "}r")} \\
  &\text{\quad (match_operand:SI 1 "memory_operand" "}m")})] \\
  &\text{""
  \\
  &\text{"lw \ t\%0, \%m1"}
  \end{align*}
  \]
  \]

- **Load Constant** \( R \leftarrow C \)

  \[
  \text{(define_insn "*constant_load"}
  \[
  \begin{align*}
  &\text{[(set (match_operand:SI 0 "register_operand" "}r")} \\
  &\text{\quad (match_operand:SI 1 "const_int_operand" "}i")})] \\
  &\text{""
  \\
  &\text{"li \ t\%0, \%c1"}
  \end{align*}
  \]
  \]
Move Operations in `spim1.md`

- **Register Move** \( R_i \leftarrow R_j \)

```lisp
(define_insn "*move_regs"
  [(set (match_operand:SI 0 "register_operand" "=r")
         (match_operand:SI 1 "register_operand" "r"))
   ""
   "move \t%0,%1"
)
```

- **Store into** \( M \leftarrow R \)

```lisp
(define_insn "*store_word"
  [(set (match_operand:SI 0 "memory_operand" "=m")
         (match_operand:SI 1 "register_operand" "r"))]
  ""
  "sw \t%1, %m0"
)
```
Code Generation in spim1 Compiler for Assignment $a = b$

- RTL statements

  (insn 7 6 8 (set (reg:SI 2 $v0 [41])
      (mem/c:SI (plus:SI (reg/f:SI 30 $fp)
          (const_int -16 [0xffffffffffffffec])))) [0 b+0 S4
      (nil))

  (insn 8 7 9 (set (mem/c:SI (plus:SI (reg/f:SI 30 $fp)
      (const_int -20 [0xfffffffffffffff0])))) [0 a+0 S4
      (reg:SI 2 $v0 [41])) test.c:10 5 *store_word
      (nil))

- Generated Code

- PRINT_OPERAND macro is called for printing the operand in right format
Code Generation in *spim1* Compiler for Assignment $a = b$

- **RTL statements**

  $\text{(insn 7 6 8 (set (reg:SI 2 $v0\ [41]))}\\\text{(mem/c:SI (plus:SI (reg/f:SI 30 $fp)\\\text{(const_int -16 [0xffffffffffffffffec])) [0 b+0 S4}}\\\text{(nil))}\\
\text{\(\text{(insn 8 7 9 (set (mem/c:SI (plus:SI (reg/f:SI 30 $fp)\\\text{(const_int -20 [0xfffffffffffffff0])) [0 a+0 S4}\\\text{(reg:SI 2 $v0\ [41])}) test.c:10 5 \ast\text{store_word}}\\\text{(nil))}$$

- **Generated Code**

  \[\text{lw\ $v0,\ -16($fp)}\]

- **PRINT_OPERAND** macro is called for printing the operand in right format
Code Generation in spim1 Compiler for Assignment $a = b$

- RTL statements

$\begin{align*}
(\text{insn} \ 7 \ 6 \ 8 \ (\text{set} \ (\text{reg:SI} \ 2 \ \$v0 \ [41])) \\
(\text{mem/c:SI} \ (\text{plus:SI} \ (\text{reg/f:SI} \ 30 \ \$fp) \\
(\text{const_int} \ -16 \ [0xffffffffffffffffec])) \ [0 \ b+0 \ S4 \\
(\text{nil})) \\
\end{align*}$

$\begin{align*}
(\text{insn} \ 8 \ 7 \ 9 \ (\text{set} \ (\text{mem/c:SI} \ (\text{plus:SI} \ (\text{reg/f:SI} \ 30 \ \$fp) \\
(\text{const_int} \ -20 \ [0xfffffffffffffffff0])) \ [0 \ a+0 \ S4 \\
(\text{reg:SI} \ 2 \ \$v0 \ [41]))) \ \text{test.c:10} \ 5 \ \text{*store_word} \\
(\text{nil}))
\end{align*}$

- Generated Code

$\begin{align*}
lw \ \$v0, \ -16(\$fp) \\
sw \ \$v0, \ -20(\$fp)
\end{align*}$

- PRINT_OPERAND macro is called for printing the operand in right format
Using register $\text{zero}$ for constant 0

- Introduce new register class `zero_register_operand` in `spim1.h` and define `move_zero`

  ```
  (define_insn "IITB_move_zero"
   [(set (match_operand:SI 0 "nonimmediate_operand" "=r,m")
       (match_operand:SI 1 "zero_register_operand" "z,z")
     )]
   ""
   "@ 
mov \t%0,%1
   sw \t%1, %m0"
  )
  ```

- How do we get `zero_register_operand` in an RTL?
Using register $\text{zero}$ for constant 0

- Use define_expand "movsi" to get zero_register_operand in an RTL
  
  if(GET_CODE(operands[1])==CONST_INT && INTVAL(operands[1])==0) {
    emit_insn(gen_IITB_move_zero(operands[0],
                                 gen_rtx_REG(SImode,0)));
    DONE;
  }
  else /* Usual processing */

- DONE says do not generate the RTL template associated with "movsi"

- required template is generated by
  emit_insn(gen_IITB_move_zero(...))
Supporting Addition in Level 1

(define_insn "addsi3"
  [(set (match_operand:SI 0 "register_operand" "+r,r")
        (plus:SI (match_operand:SI 1 "register_operand" "+r,r")
                  (match_operand:SI 2 "nonmemory_operand" "+r,i")))
   ]
  ""
  "@
   add \t%0, %1, %2
   addi \t%0, %1, %c2"
)

- Constraints combination 1 of three operands: R, R, R
- Constraints combination 2 of three operands: R, R, C
Comparing \texttt{movsi} and \texttt{addsi3}

- \texttt{movsi} uses \texttt{define\_expand} whereas \texttt{addsi3} uses combination of operands
- Why not use constraints for \texttt{movsi} too?
Comparing movsi and addsi3

- movsi uses `define_expand` whereas addsi3 uses combination of operands
- Why not use constraints for movsi too?
- Combination of operands is used during pattern matching and not during expansion
  - We will need to support memory as both source and destination
Comparing `movsi` and `addsi3`

- `movsi` uses `define_expand` whereas `addsi3` uses combination of operands.
- Why not use constraints for `movsi` too?
- Combination of operands is used during pattern matching and not during expansion.
  - We will need to support memory as both source and destination.
  - Will also allow memory to memory move in RTL.
    - We will not know until assembly emission which one is a load instruction and which one is a store instruction.
Part 5

Conclusions
Conclusions

• Incremental construction of machine description files is very instructive

• Increments in machine descriptions are governed by increments in source language

• Machine characteristics need to be specified in C macros and C functions
  ▶ Does not seem amenable to incremental construction
  ▶ Seems difficult to a novice

• Specifying instructions seems simpler and more systematic
  ▶ Is amenable to incremental construction
  ▶ The concept of minimal machine descriptions is very useful

• \texttt{define_insn} and \texttt{define_expand} are the main constructs used in machine descriptions
Part 6

Constructs Supported in Level 2
## Arithmetic Operations Required in Level 2

<table>
<thead>
<tr>
<th>Operation</th>
<th>Primitive Variants</th>
<th>Implementation</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>$Dest \leftarrow Src_1 - Src_2$</td>
<td>$R_i \leftarrow R_j - R_k$</td>
<td>sub $ri$, $rj$, $rk$</td>
<td></td>
</tr>
<tr>
<td>$Dest \leftarrow -Src$</td>
<td>$R_i \leftarrow -R_j$</td>
<td>neg $ri$, $rj$</td>
<td></td>
</tr>
<tr>
<td>$Dest \leftarrow Src_1 / Src_2$</td>
<td>$R_i \leftarrow R_j / R_k$</td>
<td>div $rj$, $rk$</td>
<td>level 2</td>
</tr>
<tr>
<td>$Dest \leftarrow Src_1 % Src_2$</td>
<td>$R_i \leftarrow R_j % R_k$</td>
<td>rem $ri$, $rj$, $rk$</td>
<td></td>
</tr>
<tr>
<td>$Dest \leftarrow Src_1 \ast Src_2$</td>
<td>$R_i \leftarrow R_j \ast R_k$</td>
<td>mul $ri$, $rj$, $rk$</td>
<td></td>
</tr>
</tbody>
</table>
# Arithmetic Operations Required in Level 2

<table>
<thead>
<tr>
<th>Operation</th>
<th>Primitive Variants</th>
<th>Implementation</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\text{Dest} \leftarrow \text{Src}_1 - \text{Src}_2$</td>
<td>$R_i \leftarrow R_j - R_k$</td>
<td>sub ri, rj, rk</td>
<td></td>
</tr>
<tr>
<td>$\text{Dest} \leftarrow -\text{Src}$</td>
<td>$R_i \leftarrow -R_j$</td>
<td>neg ri, rj</td>
<td></td>
</tr>
<tr>
<td>$\text{Dest} \leftarrow \text{Src}_1 / \text{Src}_2$</td>
<td>$R_i \leftarrow R_j / R_k$</td>
<td>div rj, rk</td>
<td>level 2</td>
</tr>
<tr>
<td>$\text{Dest} \leftarrow \text{Src}_1 % \text{Src}_2$</td>
<td>$R_i \leftarrow R_j % R_k$</td>
<td>rem ri, rj, rk</td>
<td></td>
</tr>
<tr>
<td>$\text{Dest} \leftarrow \text{Src}_1 \ast \text{Src}_2$</td>
<td>$R_i \leftarrow R_j \ast R_k$</td>
<td>mul ri, rj, rk</td>
<td></td>
</tr>
</tbody>
</table>
## Bitwise Operations Required in Level 2

<table>
<thead>
<tr>
<th>Operation</th>
<th>Primitive Variants</th>
<th>Implementation</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dest ← $\text{Src}_1 \ll \text{Src}_2$</td>
<td>$R_i \leftarrow R_j \ll R_k$</td>
<td>sllv ri, rj, rk</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$R_i \leftarrow R_j \ll C_5$</td>
<td>sll ri, rj, c</td>
<td></td>
</tr>
<tr>
<td>Dest ← $\text{Src}_1 \gg \text{Src}_2$</td>
<td>$R_i \leftarrow R_j \gg R_k$</td>
<td>srav ri, rj, rk</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$R_i \leftarrow R_j \gg C_5$</td>
<td>sra ri, rj, c</td>
<td>level 2</td>
</tr>
<tr>
<td>Dest ← $\text{Src}_1 &amp; \text{Src}_2$</td>
<td>$R_i \leftarrow R_j &amp; R_k$</td>
<td>and ri, rj, rk</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$R_i \leftarrow R_j &amp; C$</td>
<td>andi ri, rj, c</td>
<td></td>
</tr>
<tr>
<td>Dest ← $\text{Src}_1 \mid \text{Src}_2$</td>
<td>$R_i \leftarrow R_j \mid R_k$</td>
<td>or ri, rj, rk</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$R_i \leftarrow R_j \mid C$</td>
<td>ori ri, rj, c</td>
<td></td>
</tr>
<tr>
<td>Dest ← $\text{Src}_1 \wedge \text{Src}_2$</td>
<td>$R_i \leftarrow R_j \wedge R_k$</td>
<td>xor ri, rj, rk</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$R_i \leftarrow R_j \wedge C$</td>
<td>xori ri, rj, c</td>
<td></td>
</tr>
<tr>
<td>Dest ← $\overline{\text{Src}}$</td>
<td>$R_i \leftarrow \overline{R_j}$</td>
<td>not ri, rj</td>
<td></td>
</tr>
</tbody>
</table>
Divide Operation in spim2.md using define_insn

- For division, the spim architecture imposes use of multiple asm instructions for single operation.

```
(define_insn "divsi3"
  [(set (match_operand:SI 0 "register_operand" ";=r")
        (div:SI (match_operand:SI 1 "register_operand" "r")
                (match_operand:SI 2 "register_operand" "r")))
   
   "\tdiv\t%1, %2\n\tmflo\t%0"
)
```
Divide Operation in spim2.md using define_insn

- For division, the spim architecture imposes use of multiple asm instructions for single operation.
- Two ASM instructions are emitted using single RTL pattern

```
(define_insn "divsi3"
 [(set (match_operand:SI 0 "register_operand" ";=r")
   (div:SI (match_operand:SI 1 "register_operand" ";r")
     (match_operand:SI 2 "register_operand" ";r")))
 ]]

""

"div\t%1, %2\n\tmflo\t%0"
```

Essential Abstractions in GCC
GCC Resource Center, IIT Bombay
Advantages/Disadvantages of using `define_insn`

- Very simple to add the pattern
- Primitive target feature represented as single insn pattern in `.md`
- Unnecessary atomic grouping of instructions
- May hamper optimizations in general, and instruction scheduling, in particular
The RTL pattern can be expanded into two different RTLs.

```
(define_expanded "divsi3"
  [(parallel
    [(set (match_operand:SI 0 "register_operand" "")
      (div:SI (match_operand:SI 1 "register_operand" "")
        (match_operand:SI 2 "register_operand" ""))]
    (clobber (reg:SI 26))
    )]
  )
)
```

```
{"emit_insn(gen_IITB_divide(gen_rtx_REG(SImode,26),
  operands[1], operands[2]));
emit_insn(gen_IITB_move_from_lo(operands[0],
  gen_rtx_REG(SImode,26)));
DONE;"}
)
Divide Operation in `spim2.md` using `define_expand`

- Divide pattern equivalent to div instruction in architecture.

```
(define_insn "IITB_divide"
  [(parallel[(set (match_operand:SI 0 "LO_register_operand" 
    
"=q") (div:SI (match_operand:SI 1 "register_operand" 
      
"r")
      
(match_operand:SI 2 "register_operand" 
      "r"))
      
(clobber (reg:SI 27))]))]
  ""
  "div t%1, %2"
)
```
Divide Operation in `spim2.md` using `define_expand`

- Divide pattern equivalent to div instruction in architecture.

```
(define_insn "IITB_divide"
  [(parallel
     [(set (match_operand:SI 0 "Lo_register_operand" ";=q")
       (div:SI (match_operand:SI 1 "register_operand" "r")
       (match_operand:SI 2 "register_operand" "r")))
     ]
   )
   (clobber (reg:SI 27)))
   ""
   "div t%1, %2"
)```

Essential Abstractions in GCC

GCC Resource Center, IIT Bombay
Divide Operation in spim2.md using define_expand

- Moving contents of special purpose register LO to/from general purpose register

```lisp
(define_insn "IITB_move_from_lo"
  [(set (match_operand:SI 0 "register_operand" "=r")
       (match_operand:SI 1 "LO_register_operand" "q"))]
  ""
  "mflo \t%0"
)

(define_insn "IITB_move_to_lo"
  [(set (match_operand:SI 0 "LO_register_operand" "=q")
       (match_operand:SI 1 "register_operand" "r"))]
  ""
  "mtlo \t%1"
)
```
Divide Operation in \texttt{spim2.md} using \texttt{define\_expand}

- Divide pattern equivalent to div instruction in architecture.

```markdown
(define_insn "modsi3"
  [(parallel
     [(set (match_operand:SI 0 "register_operand" ";=r")
       (mod:SI (match_operand:SI 1 "register_operand" "r")
       (match_operand:SI 2 "register_operand" "r")))
     (clobber (reg:SI 26))
     (clobber (reg:SI 27))]
   ""
   "rem \t%0, %1, %2"
)
```

Divide Operation in `spim2.md` using `define_expand`

- Divide pattern equivalent to div instruction in architecture.

```lisp
(define_insn "modsi3"
  [(parallel
     [(set (match_operand:SI 0 "register_operand" ";=r")
       (mod:SI (match_operand:SI 1 "register_operand" ";r")
        (match_operand:SI 2 "register_operand" ";r")))
     (clobber (reg:SI 26))
     (clobber (reg:SI 27)))]
  ""
  "rem \t%0, %1, %2"
)
```

Essential Abstractions in GCC

GCC Resource Center, IIT Bombay
Advantages/Disadvantages of Using `define_expand for Division`

- Two instructions are separated out at GIMPLE to RTL conversion phase
- Both instructions can undergo all RTL optimizations independently
- C interface is needed in md
- Compilation becomes slower and requires more space
Divide Operation in `spim2.md` using `define_split`

```latex
(define_split
 [(parallel [(set (match_operand:SI 0 "register_operand" "")
 (div:SI (match_operand:SI 1 "register_operand" "")
 (match_operand:SI 2 "register_operand" "")))
 )
 (clobber (reg:SI 26))
 (clobber (reg:SI 27))])]
"

[(parallel [(set (matchDup 3)
 (div:SI (matchDup 1)
 (matchDup 2)))
 (clobber (reg:SI 27))])
 (set (matchDup 0)
 (matchDup 3))
]

"operands[3]=gen_rtx_REG(SImode,26); "
```

Essential Abstractions in GCC

GCC Resource Center, IIT Bombay
(define_split
  [(parallel [(set (match_operand:SI 0 "register_operand" "")
                (div:SI (match_operand:SI 1 "register_operand" ")
                (match_operand:SI 2 "register_operand" "")
                )]
           (clobber (reg:SI 26))
           (clobber (reg:SI 27))]]
  ""
[(parallel [(set (match_dup 3)
               (div:SI (match_dup 1)
               (match_dup 2))]
           (clobber (reg:SI 27)))]
  (set (match_dup 0)
       (match_dup 3))
"
"operands[3]=gen_rtx_REG(SImode,26); "
)
(define_split
[(parallel [(set (match_operand:SI 0 "register_operand" "")
    (div:SI (match_operand:SI 1 "register_operand" ")
    (match_operand:SI 2 "register_operand" "")
    )
    (clobber (reg:SI 26))
    (clobber (reg:SI 27)))])
"
]
[(parallel [(set (match_dup 3)
    (div:SI (match_dup 1)
    (match_dup 2)))
    (clobber (reg:SI 27)))])
(set (match_dup 0)
    (match_dup 3))
]
"operands[3]=gen_rtx_REG(SImode,26); "
)
Part 7

Constructs Supported in Level 3
## Operations Required in Level 3

<table>
<thead>
<tr>
<th>Operation</th>
<th>Primitive Variants</th>
<th>Implementation</th>
<th>Remark</th>
</tr>
</thead>
</table>
| $Dest \leftarrow \text{fun}(P_1, \ldots, P_n)$ | call $L_{\text{fun}}, n$ | $\text{l}w \ r_i, [\text{SP}+c1]$  
$\text{sw} \ r_i, [\text{SP}]$  
:  
$\text{l}w \ r_i, [\text{SP}+c2]$  
$\text{sw} \ r_i, [\text{SP}-n*4]$  
jal $L$ | Level 1 |
| $\text{fun}(P_1, P_2, \ldots, P_n)$  | call $L_{\text{fun}}, n$ | $\text{l}w \ r_i, [\text{SP}+c1]$  
$\text{sw} \ r_i, [\text{SP}]$  
:  
$\text{l}w \ r_i, [\text{SP}+c2]$  
$\text{sw} \ r_i, [\text{SP}-n*4]$  
jal $L$ | Level 1 |

New
(define_insn "call"
  [(call (match_operand:SI 0 "memory_operand" "=m")
        (match_operand:SI 1 "immediate_operand" "i"))
   (clobber (reg:SI 31))
  ]
  ""
  "*
   return emit_asm_call(operands,0);
  "
 )
Call Operation in spim3.md

(define_insn "call_value"
 [(set (match_operand:SI 0 "register_operand" "+=r")
       (call (match_operand:SI 1 "memory_operand" "+m")
       (match_operand:SI 2 "immediate_operand" "+i")))
  (clobber (reg:SI 31))
]"
"
"*
   return emit_asm_call(operands,1);
"
)
Activation Record Generation during Call

- Operations performed by caller

- Operations performed by callee
Activation Record Generation during Call

- Operations performed by caller

- Operations performed by callee
Activation Record Generation during Call

- Operations performed by caller
  - Push parameters on stack.

- Operations performed by callee

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- Operations performed by callee

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- Operations performed by caller
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**Activation Record Generation during Call**

- **Operations performed by caller**
  - Push parameters on stack.

- **Operations performed by callee**

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Activation Record Generation during Call

- Operations performed by caller
  - Push parameters on stack.
  - Load return address in return address register.

- Operations performed by callee

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Activation Record Generation during Call

- Operations performed by caller
  - Push parameters on stack.
  - Load return address in return address register.
  - Transfer control to Callee.
- Operations performed by callee

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Activation Record Generation during Call

- Operations performed by caller
  - Push parameters on stack.
  - Load return address in return address register.
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- Operations performed by callee
  - Push Return address stored by caller on stack.

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## Activation Record Generation during Call

### Operations performed by caller
- Push parameters on stack.
- Load return address in return address register.
- Transfer control to Callee.

### Operations performed by callee
- Push Return address stored by caller on stack.
- Push caller’s Frame Pointer Register.

### Caller’s Activation Record
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  - Save callee saved registers, if used by callee.

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  - Save callee saved registers, if used by callee.
  - Create local variables frame.

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<td>Local Variable 2</td>
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Activation Record Generation during Call

- Operations performed by caller
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<td>Local Variable ( n )</td>
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Activation Record Generation during Call

- Operations performed by caller
  - Push parameters on stack.
  - Load return address in return address register.
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- Operations performed by callee
  - Push Return address stored by caller on stack.
  - Push caller’s Frame Pointer Register.
  - Push caller’s Stack Pointer.
  - Save callee saved registers, if used by callee.
  - Create local variables frame.
  - Start callee body execution.

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</tr>
<tr>
<td>...</td>
</tr>
<tr>
<td>Local Variable $n$</td>
</tr>
</tbody>
</table>
(define_expand "prologue"
  [(clobber (const_int 0))]
  ""
  {
    spim_prologue();
    DONE;
  })
(define_expand "prologue"
[(clobber (const int 0))]
"
{
  spim_prologue();
  DONE;
}
)
Epilogue in spim3.md

```
(define_expand "epilogue"
  [(clobber (const_int 0))]
  ""

  spim_epilogue();
  DONE;
)
```

```
(set (reg:SI $sp)
  (reg:SI $fp))

(set (reg:SI $fp)
  (mem:SI (plus:SI (reg:SI $sp)
    (const_int -8 ))))

(set (reg:SI $ra)
  (mem:SI (reg:SI $sp)))

(parallel [
  (return)
  (use (reg:SI $ra))])
```
Part 8

Constructs Supported in Level 4
# Operations Required in Level 4

<table>
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<tr>
<th>Operation</th>
<th>Primitive Variants</th>
<th>Implementation</th>
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</table>
| $Src_1 < Src_2 ?$  
goto L : PC | $CC \leftarrow R_i < R_j$
$CC < 0 ?$ goto L : PC | blt $r_i, r_j, L$ |
| $Src_1 > Src_2 ?$  
goto L : PC | $CC \leftarrow R_i > R_j$
$CC > 0 ?$ goto L : PC | bgt $r_i, r_j, L$ |
| $Src_1 \leq Src_2 ?$  
goto L : PC | $CC \leftarrow R_i \leq R_j$
$CC \leq 0 ?$ goto L : PC | ble $r_i, r_j, L$ |
| $Src_1 \geq Src_2 ?$  
goto L : PC | $CC \leftarrow R_i \geq R_j$
$CC \geq 0 ?$ goto L : PC | bge $r_i, r_j, L$ |
# Operations Required in Level 4

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| $Src_1 == Src_2$ ? goto L : PC | $CC \leftarrow R_i == R_j$
$CC == 0 ? goto L : PC | beq $r_i, r_j, L$ |          |
| $Src_1 \neq Src_2$ ? goto L : PC | $CC \leftarrow R_i \neq R_j$
$CC \neq 0 ? goto L : PC | bne $r_i, r_j, L$ |          |
(define_insn "cbranchsi4"
  [(set (pc)
       (if_then_else
        (match_operator 0 "comparison_operator"
          [(match_operand:SI 1 "register_operand" "")
           (match_operand:SI 2 "register_operand" "")])
        (label_ref (match_operand 3 "" "")
          (pc)))]
   ""
   "*
    return conditional_insn(GET_CODE(operands[0]),operands);
   "
  )
Support for Branch pattern in spim4.c

```c
char *
conditional_insn (enum rtx_code code, rtx operands[])
{
    switch(code)
    {
        case EQ:return "beq %1, %2, %l3";
        case NE:return "bne %1, %2, %l3";
        case GE:return "bge %1, %2, %l3";
        case GT:return "bgt %1, %2, %l3";
        case LT:return "blt %1, %2, %l3";
        case LE:return "ble %1, %2, %l3";
        case GEU:return "bgeu %1, %2, %l3";
        case GTU:return "bgtu %1, %2, %l3";
        case LTU:return "bltu %1, %2, %l3";
        case LEU:return "bleu %1, %2, %l3";
        default: /* Error. Issue ICE */
    }
}
```
Alternative for Branch: Conditional compare in spim4.md

```
(define_code_iterator cond_code
    [lt ltu eq ge geu gt gtu le leu ne])

(define_expand "cmpsi"
    [(set (cc0) (compare
        (match_operand:SI 0 "register_operand" ")")
        (match_operand:SI 1 "nonmemory_operand" ")")))

"

{
    compare_op0=operands[0];
    compare_op1=operands[1];
    DONE;
}
```

(define_expand "b<code>"
[(set (pc) (if_then_else (cond_code:SI (match_dup 1)
  (match_dup 2))
  (label_ref (match_operand 0 "" ""))
  (pc)))]
"
{
  operands[1]=compare_op0;
  operands[2]=compare_op1;
  if(immediate_operand(operands[2],SImode))
  {
  }
}
)
Alternative for Branch: Branch pattern in spim4.md

(define_insn "*insn_b<code>"
   [(set (pc)
       (if_then_else
         (cond_code:SI
           (match_operand:SI 1 "register_operand" "r")
           (match_operand:SI 2 "register_operand" "r")))
         (label_ref (match_operand 0 "" ""))
         (pc))])
   ""
   "*

   return conditional_insn(<CODE>,operands);
   ""
)