CS-292 Project Report

DATA ROUTER

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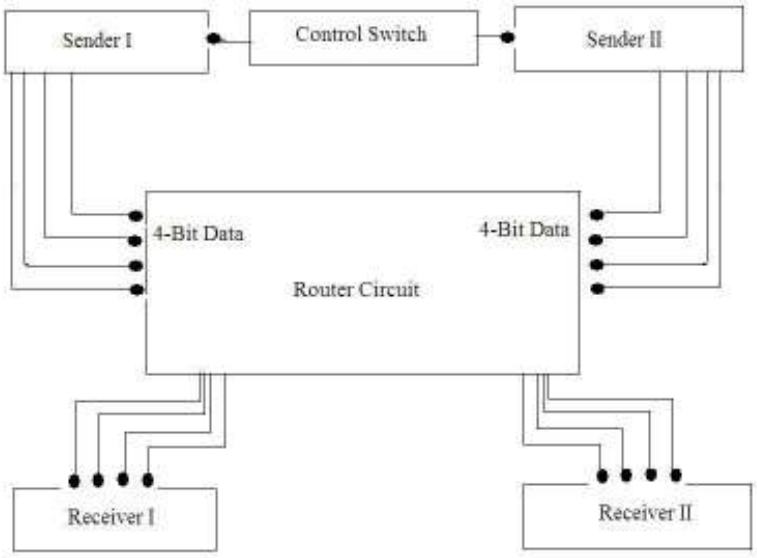
Introduction

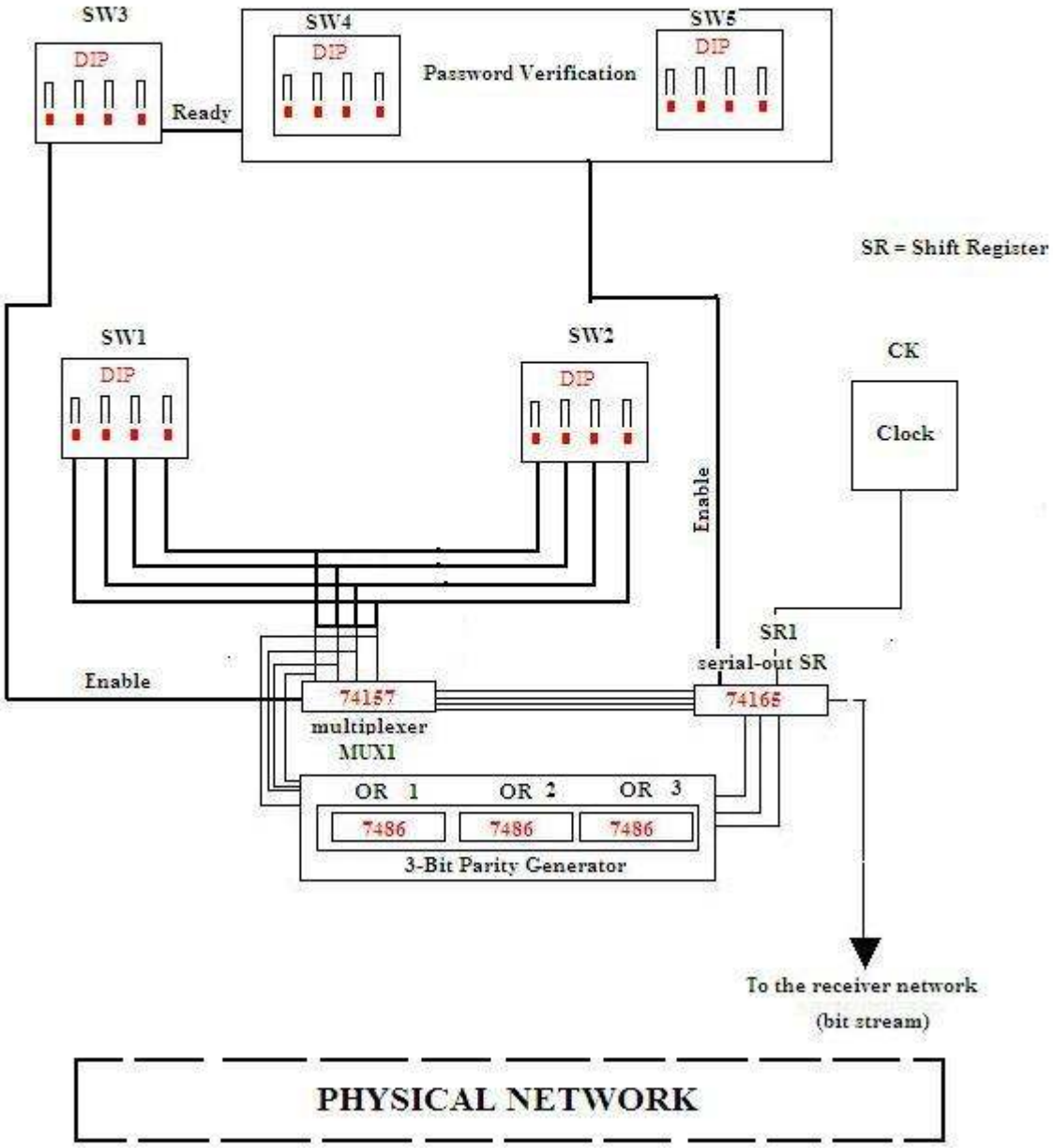
This project aims at simulating a data router serving multiple (n) clients acting as data sources/senders and multiple (m) prospective receivers.

A detailed Description with schematic diagram is given below:

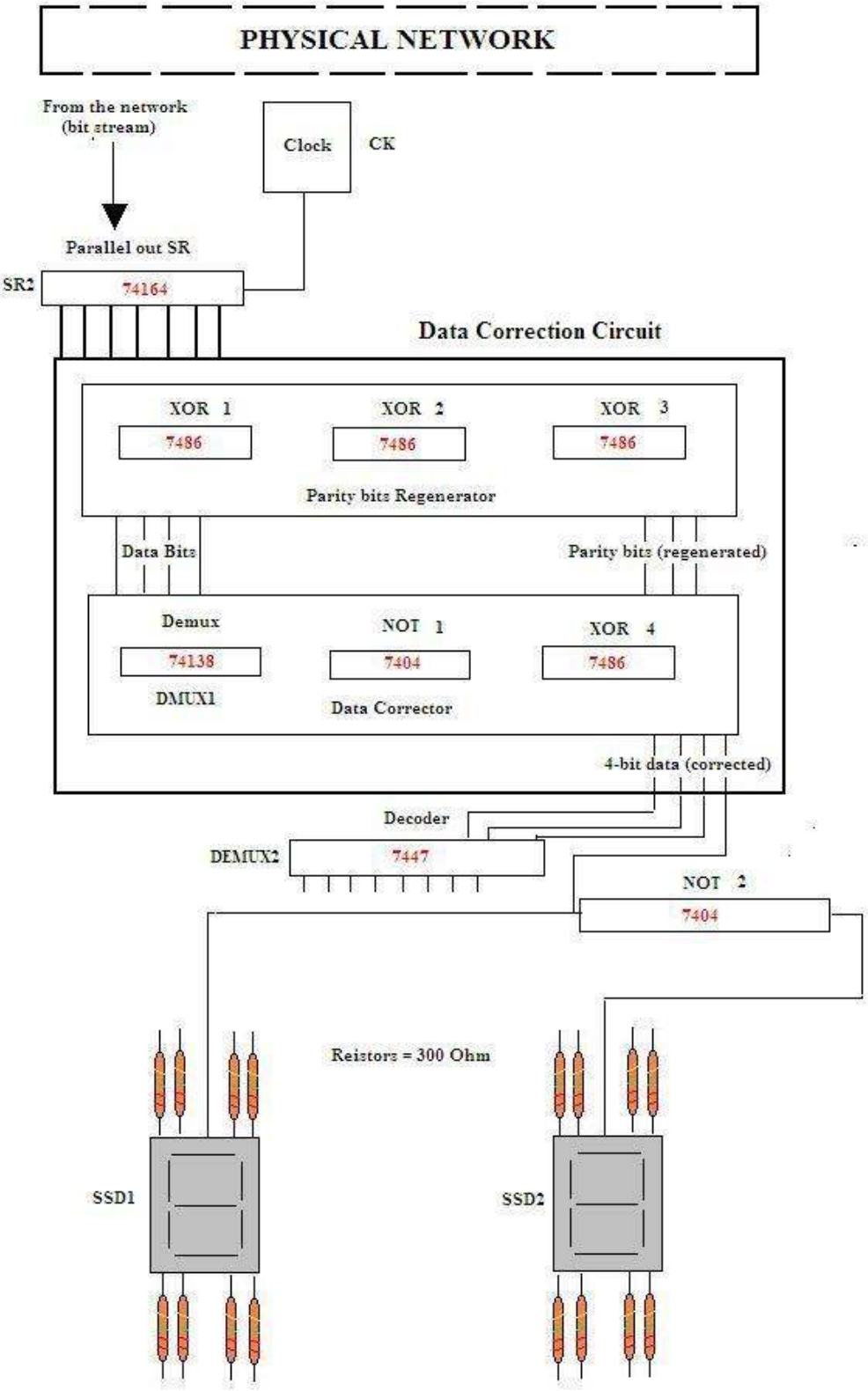
Detailed Description with schematic diagram:

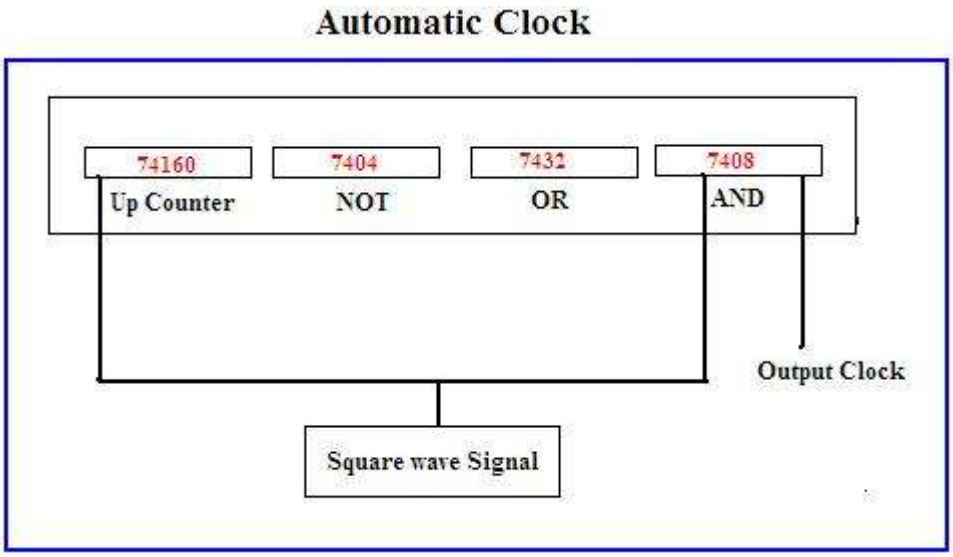


Sender Side


SW3
DIP
Ready
SW4
DIP
Password Verification
SW5
DIP
SR = Shift Register
SW1
DIP
SW2
DIP
CK
Clock
Enable
SR1
serial-out SR
Enable
74157
multiplexer
MUX1
74165
OR 1
OR 2
OR 3
7486
7486
7486
3-Bit Parity Generator
To the receiver network
(bit stream)
PHYSICAL NETWORK

Receiver Side





Functional Description:

This project aims at simulating a data router serving multiple (n) clients acting as data sources/senders and multiple (m) prospective receivers.

The system has been provided with global control for choosing one out of the n possible senders and each chosen sender has been given options to specify the receiver to which the data is sent besides the data itself.

Two more functionalities, as mentioned in the project proposal have been added:

- Detection and correction of error in the data during transfer
- Basic user authentication (password based)

In our prototype the values have been limited as follows:

- Number of possible senders (n) : 2
- Number of possible receivers (m) : 2

- Amount of data transferred : 3 bits
- Maximum error handling capacity : 1 bit

The global (or administrator) control switch (SW3) is set to decide which user is sending his data.

The data is then loaded on to a parallel load-serial shift register SR1 (IC 74165)using the multiplexer MUX1 (IC 74157).
Meanwhile the Parity bits generator circuit component generates 3 parity bits and inserts them into their correct position in the data stream. This makes the total number of bits to be sent over the network to be 7 (4 data bits + 3 parity bits).
Now the SW3 port 1 is set to indicate that the system is now ready to transfer the data. The password is set on SW4 and the data is sent only if this matches the originally set password on SW5.
Data in the shift register SR1 now moves out into the bit-stream with each clock pulse. After 7 such clock pulses all the data in SR1 gets flushed into the network.
On the receiver side 7 pulses cause the data to get loaded into the serial load-parallel out shift register SR2 (IC 74164).
The 7 received bits are then fed into the data correction circuit.
This circuit has two components.
The first component generates fours new parity bits and the second one corrects the data if the first component indicates that there has indeed been some error in data transmission.
Out of the corrected 4 bits the first least significant three bits (which constitute the 'actual message') are then sent to a decoder connected to the Seven Segment Displays of both the receivers (SSD1 and SSD2).
The last bit which is the address bit is then used to decide that which user actually displays the data.

User Scenario Description:

There are two senders and receivers in the network. There is a network administrator who decides which sender is allowed to send his 3 bit data when the data is ready. This is controlled by the switch SW3. The port4 selects the sender. Port4 ON means sender1 (sw1) is sending the data, else

sender2 (SW2). The Port1 OFF means the data is still not ready, else the data is ready to be sent.
In addition to this both the user need to give a network password (using SW4). The network password can be set using SW5. If both the password match only then the user N is allowed to transfer his data.
Both the users send three bit data using Ports 1, 2 and 3 (in ascending order of significance) and one bit (Port 4) for sender address. Port ON means bit 0 else 1.
Let the 4 bits be: “0110” (the first being the LSB in order).
So we have the message “011” and the receiver set to 0 (the last bit).
This input bit-stream is then sent over the network and the decimal number corresponding to the three bit data is displayed to the corresponding receiver.
On the receiver side the address bit (Port 4 = 0) is used to decide which receiver gets the data and the other three bits, the ‘actual data’ or the ‘message’ is displayed to the correct receiver (receiver 0).
So finally the Seven Segment display of receiver 0 will display 6 (== “110”).