# Timed systems through the lens of logic

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# A global view of timed systems

**A timed system has several parts:**

1. A regular way to generate behaviors: Automata, Expressions
2. Timing features: Clock resets and guards, Event-clocks, Clock updates etc.

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**Examples**

- Timed automata, event clock automata AD94,AFH99
- Timed pushdown automata BER94,AAS12
- Timed message-passing automata AGKS10,AAK18

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- Popular approach: region construction. For each timing feature and each data structure, redo the proof.
- Do we need to do this? Is there something unifying them?

# A unifying graphical view

- A run of system $S$ is a sequence of instructions
  - e.g., with a queue $d_1$ and stack $d_2$ consider

    $\tau = \text{nop}\ w(d_1)\ \text{nop}\ w(d_1)\ r(d_1)\ w(d_2)\ w(d_2)\ r(d_1)\ \text{nop}\ r(d_2)\ r(d_2)$

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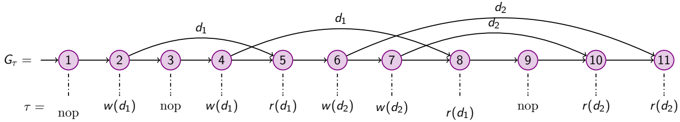
- Gives rise to a node and edge-labeled graph $G_\tau$



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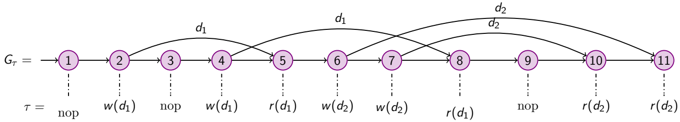

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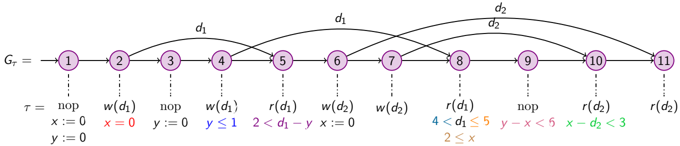

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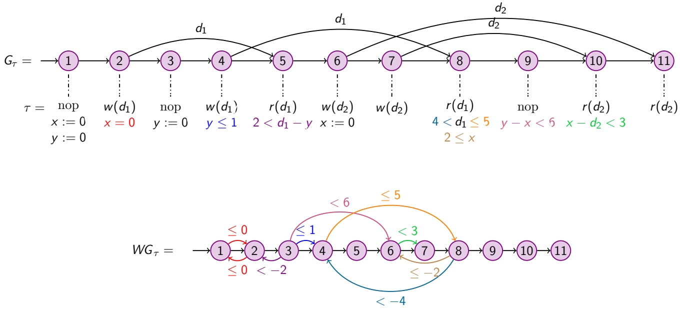
- A run must be realizable, i.e., weighted graph $WG_\tau$ should not have negative cycle!



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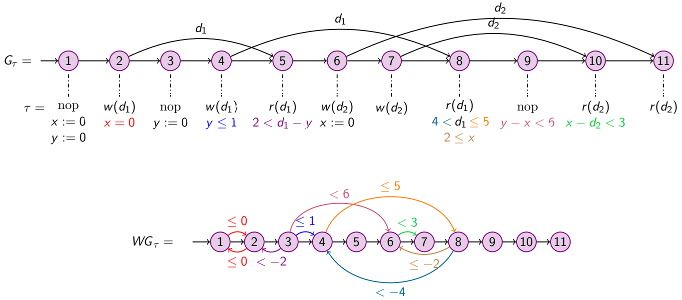


So emptiness asks if there exists $\tau$ generated by $S$ such that

(i) $G_\tau$ is valid and (ii) $WG_\tau$ is realizable?

# Related work

## Untimed setting- Use Courcelle's theorem

MP11,AKG12,AG14

- Show that graphs $G_\tau$ obtained have bounded tree-width
- Write validity in MSO over these graphs $G_\tau$
- Interpret these graphs over trees, and reduce to emptiness of tree automata

Main questions:

- Is realizability MSO definable?
- Do timed graphs $WG_\tau$ have bounded tree-width?
- Can you avoid the complexity blowup?

# Related work (contd.)

## Timed setting - for TPDA and restricted TMPDA

AGK16,AGKS17,AGK18

- Show that timed graphs from TPDA have bounded tree-width
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Main question:

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## Orthogonal technique for TA, TPDA

Encoding as registers and going via atoms CL15,CLLM17,CL18

# Our results

**Theorem**

Realizability of weighted graphs is MSO (and EQ-ICPDL) definable iff the set of graphs has width 1.

- width is the size of the largest antichain
- width=1 implies linear order, i.e., graphs coming from sequential systems.

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## A template to analyze timed systems via graphs and logic

1. Timed systems to Graphs
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   - A challenge: how do we relate the decoupled graphs?

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**Theorem**

Emptiness of timed system can be reduced to satisfiability of formula in MSO/EQ-ICPDL

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   - under-approximate approach to decidability of emptiness.
   - e.g., if tree-width is bounded, then interpret these graphs in trees and obtain tree automata.

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**Extensions: Capture rich timing interplay & model checking**

# What logic shall we use?

## Propositional dynamic logic with Intersection & Converse(ICPDL)

We have the following, with $p \in \Sigma$ and $\gamma \in \Gamma$:

$$\Phi ::= \mathsf{E}\,\sigma \;:\; \neg\Phi \;:\; \Phi \vee \Phi$$

$$\sigma ::= \top \;:\; p \;:\; \sigma \vee \sigma \;:\; \neg\sigma \;:\; \langle\pi\rangle\sigma \;:\; \mathsf{loop}(\pi)$$

$$\pi ::= \xrightarrow{\gamma} \;:\; \mathsf{test}\{\sigma\} \;:\; \pi + \pi \;:\; \pi \cdot \pi \;:\; \pi^* \;:\; \pi^{-1} \;:\; \pi \cap \pi$$

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- $\Phi$ are sentences, $E$ existential node quantifier.
- $\sigma$ node or state formulae with one (implicit) free FOvar
- $\pi$ path or program formulae with two (implicit) free FOvar

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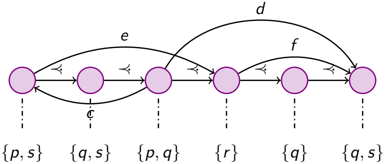


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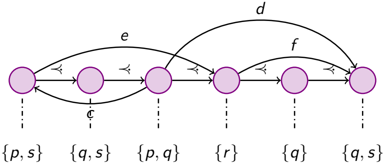


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$\mathsf{E}\,\langle(\mathrm{test}\{p \vee q\} \cdot \xrightarrow{\prec})^{*}\rangle r$

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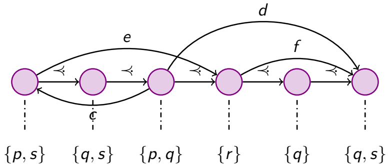


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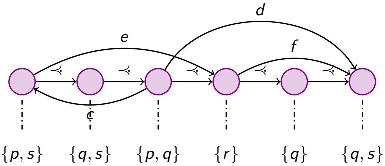


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## EQ-ICPDL($\Sigma, \Gamma$) allows $\exists$-quant over new propositional variables

$\Psi = \exists p_1, \ldots, p_n\ \Phi$ where $AP = \{p_1, \ldots, p_n\}$ is disjoint from $\Sigma$ and $\Phi \in ICPDL(\Sigma \uplus AP, \Gamma)$.

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- The following theorem by Göller, Lohrey, Lutz

## Theorem [GLL09]

Given $k \geq 1$ in unary and a formula $\Psi$ in EQ-ICPDL$(\Sigma, \Gamma)$ of intersection width bounded by a constant, checking whether $G \models \Psi$ for some $(\Sigma, \Gamma)$-labeled graph $G$ whose tree-width is at most $k$ can be solved in EXPTIME.

# Solving realizability by modulo counting

**$G$ is realizable**

iff $\exists ts : V \to \mathbb{R}$ s.t

- $\forall u \curvearrowright^{a} v, ts(v) - ts(u) \leq a$
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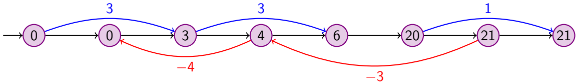
$M = 5$



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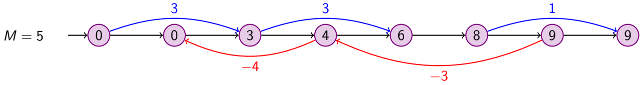

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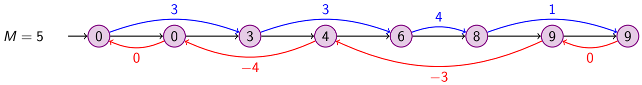

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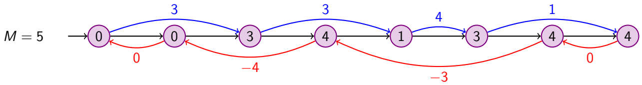


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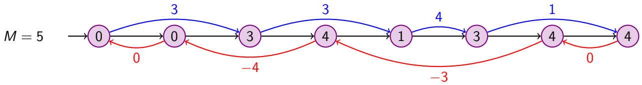


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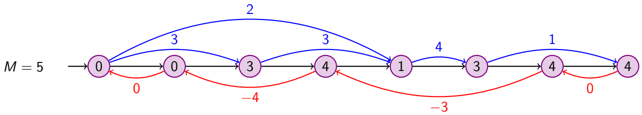


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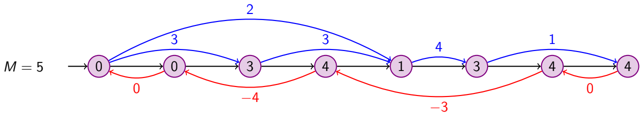


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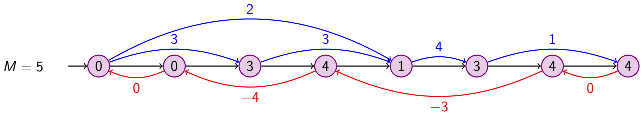


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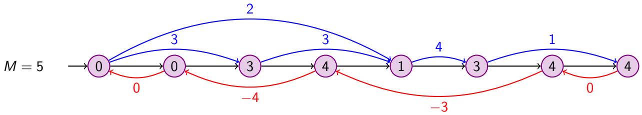
# Solving realizability by modulo counting

**Assume only closed guards: $G$ is realizable**

iff $\exists ts : V \to \mathbb{N}$ s.t $\forall u \curvearrowright^{a} v, ts(v) - ts(u) \leq a$.

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$(u, v)$ is big if $\exists u \prec w \prec x \preceq v$ s.t

$$(tsm(w) - tsm(u))[M] + (tsm(x) - tsm(w))[M] \geq M$$

# Writing it in EQ-ICPDL

Realizable iff $\exists tsm : V \to \{0, \ldots M-1\}$ s.t $\forall u \curvearrowright^{a} v$,

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$$\text{BigPath} = \sum_{\substack{0 \leq i,j,k < M \\ (j-i)[M]+(k-j)[M] \geq M}} \text{test}\{p_i\} \cdot \to^{+} \cdot \text{test}\{p_j\} \cdot \to^{+} \cdot \text{test}\{p_k\} \cdot \to^{*}$$

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$$(u, v)\text{is not big} = \neg \mathrm{E} \bigvee_{-M < \alpha < M} \mathrm{loop}(\mathrm{BigPath} \cdot \xrightarrow{\leq \alpha}{}^{-1})$$

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$$\text{Realizable} = \exists p_1, \ldots, p_{M-1}\ \text{Partition} \wedge \text{Forward} \wedge \text{Backward}$$

$$\text{Partition} = \mathsf{A} \bigvee_{0 \leq i < M} [p_i \wedge \bigwedge_{j \neq i} \neg p_j]$$

$$\text{Forward} = \neg \mathsf{E} \bigvee_{-M < \alpha < M} \text{loop}(\text{BigPath} \cdot \xrightarrow{\leq \alpha}{}^{-1}) \wedge \neg \mathsf{E} \bigvee_{\substack{0 \leq i, j < M \\ (j-i)[M] > \alpha}} \text{loop}(\text{test}\{p_i\} \cdot \xrightarrow{\leq \alpha} \cdot \text{test}\{p_j\} \cdot (\to^{-1})^{+})$$

Similarly for Backward, but need to define $\neg$BigPath (see paper)

# What about strict/open guards

**What happens when there are both closed and open guards?**

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## Capturing strict guards

- Consider the orderings of fractional parts.
- These should not form a cycle which a strict constraint within!
- Uses intersection (but with intersection-width 2).

Realizable $= \exists p_1, \ldots, p_{M-1}$ Partition $\wedge$ Forward $\wedge$ Backward $\wedge$ noFracCycle

# Realizability is not MSO definable without the linear order

- Width of a partial order = maximal size of anti-chain.
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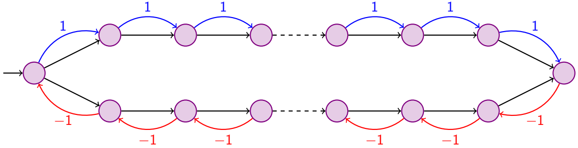

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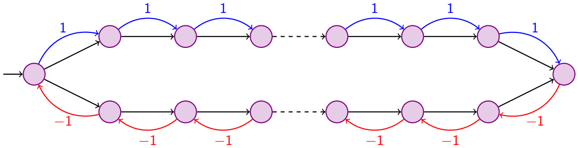

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- Width of a partial order $=$ maximal size of anti-chain.
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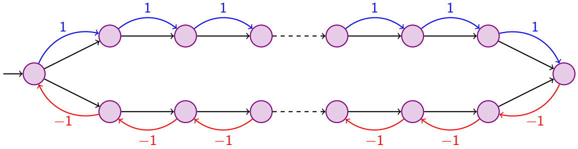
- Consider the following example with width 2.
- The graph is realizable iff #blue edges is $\geq$ #red edges.
- Cannot be expressed in MSO (formal proof by backward translation).



# Application and extensions

**A two step template to capture rich timing features**

- Capture timing as edges on graph
- Relate the events in logic

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Example: event-clock $next_a$

- edge between current event and next occurrence of a.

$$\sum_{a \in AP} \mathrm{test}\{(\mathrm{next}_a \lhd \alpha)\} \cdot \to \cdot (\mathrm{test}\{\neg a\} \cdot \to)^* \cdot \mathrm{test}\{a\}$$

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## A two step template to capture rich timing features

- Capture timing as edges on graph
- Relate the events in logic

Clock tracking/renaming

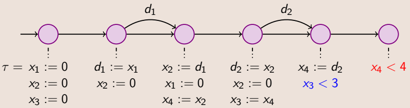


Figure: Intricate flow of information in complex updates.

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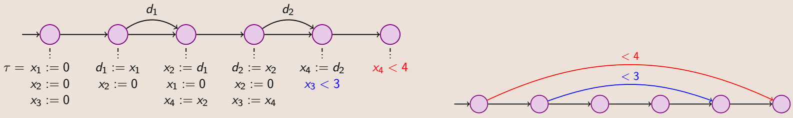


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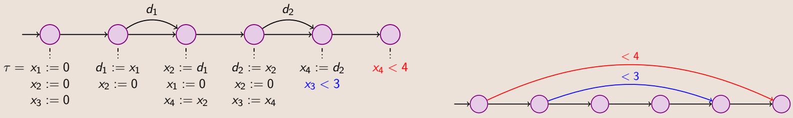


Figure: Intricate flow of information in complex updates.

## More in the paper: Model checking

Untimed and some limited timed specifications.

# Conclusion

## Highlights

- Realizability is MSO definable over sequential systems
- Template for analyzing rich time features in systems with data structures using graphs and logic
- Use EQ-ICPDL instead of MSO to obtain good complexity

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## Future work

- More consequences and applications.
- Distributed systems.
- A converse characterization?!