

**INDIAN INSTITUTE OF TECHNOLOGY, BOMBAY**  
**DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING**

**Mid-Semester Examination**

Course No. : CS 330

Day : Friday

Course Name: Microprocessor & Interfaces

Date : 25<sup>th</sup> February 2005

Marks : 30

Time : 2:30 to 4:30 p.m.

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1. Can you identify to which standard interface the following signals belong and what function they perform? [6]

a. AUTO FeedXT : Centronix

With this signal being at "LOW" level, the paper fed one line after printing. (The signal level can be fixed to "LOW" with DIP SW PIN 2-3 provided on the control circuit board).

b. CD : RS232  
RECEIVED LINE SIGNAL DETECTOR

c. DSR : RS 232  
DATA SET READY

d. ACKNLG : Centronix

Approximately 5  $\mu$ s pulse; "LOW" indicates that data has been received and the printer is ready to accept other data.

e. SLCT-OUT: Centronix  
The signal indicates that the printer is in selected state.

f. ERROR : Centronix  
The level of a signal becomes "LOW" when the printer is in "PAPER END" state, "OFFLINE" state and "ERROR" state.

2. Briefly give the protocol in the standard RS232 interface for a full duplex operation. Clearly show the sequence of operations. [4]

**RS232 PROTOCOL**

**DTR** After the terminal is turned on and terminal runs any self checks, this signal is asserted to tell the modem it is ready.

**DSR** Is asserted when the modem is ready to transmit or receive

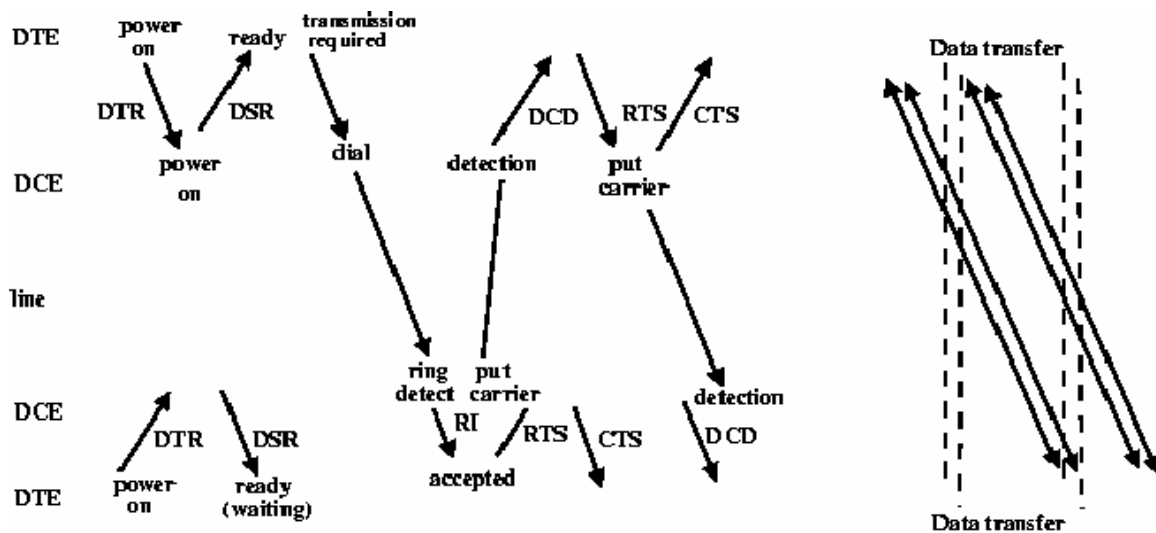
data.

- RTS Asserted by the terminal when it is ready to send a character.
  - CD Asserted by Modem to indicate that it has established contact with computer.
  - CTS Asserted when modem is fully ready to transmit data.
- Terminal then sends serial data to modem
- RTS Deasserted to indicate all characters have been sent.
  - CTS Modem deasserts and stops transmission.

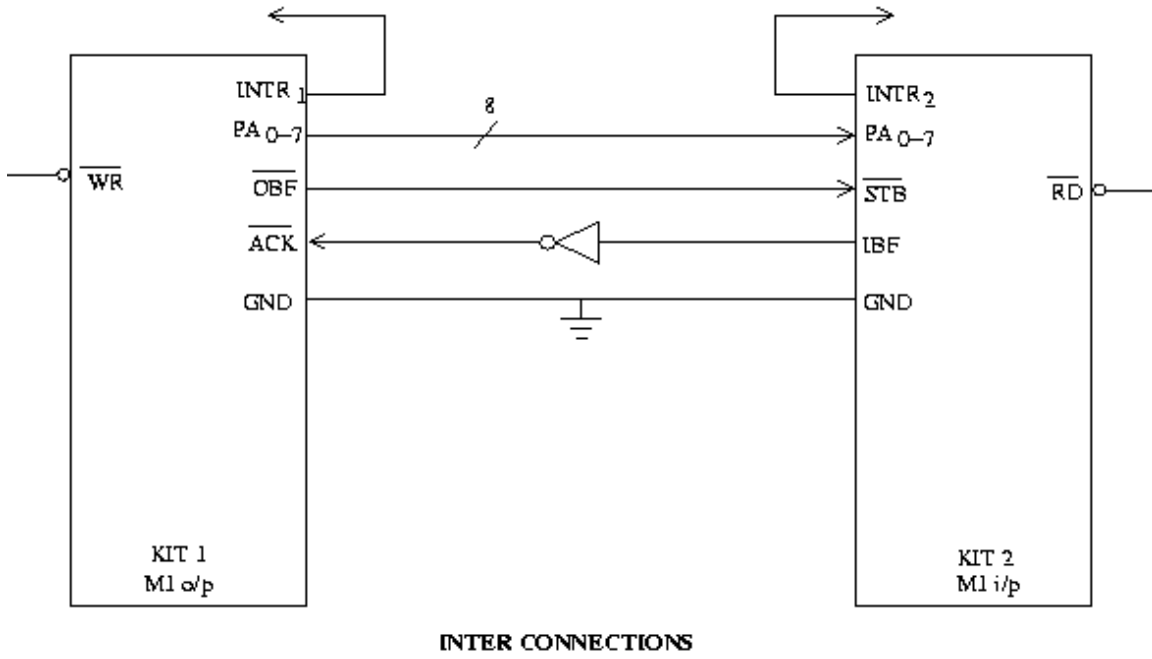
### **DTE-DTE Connection**

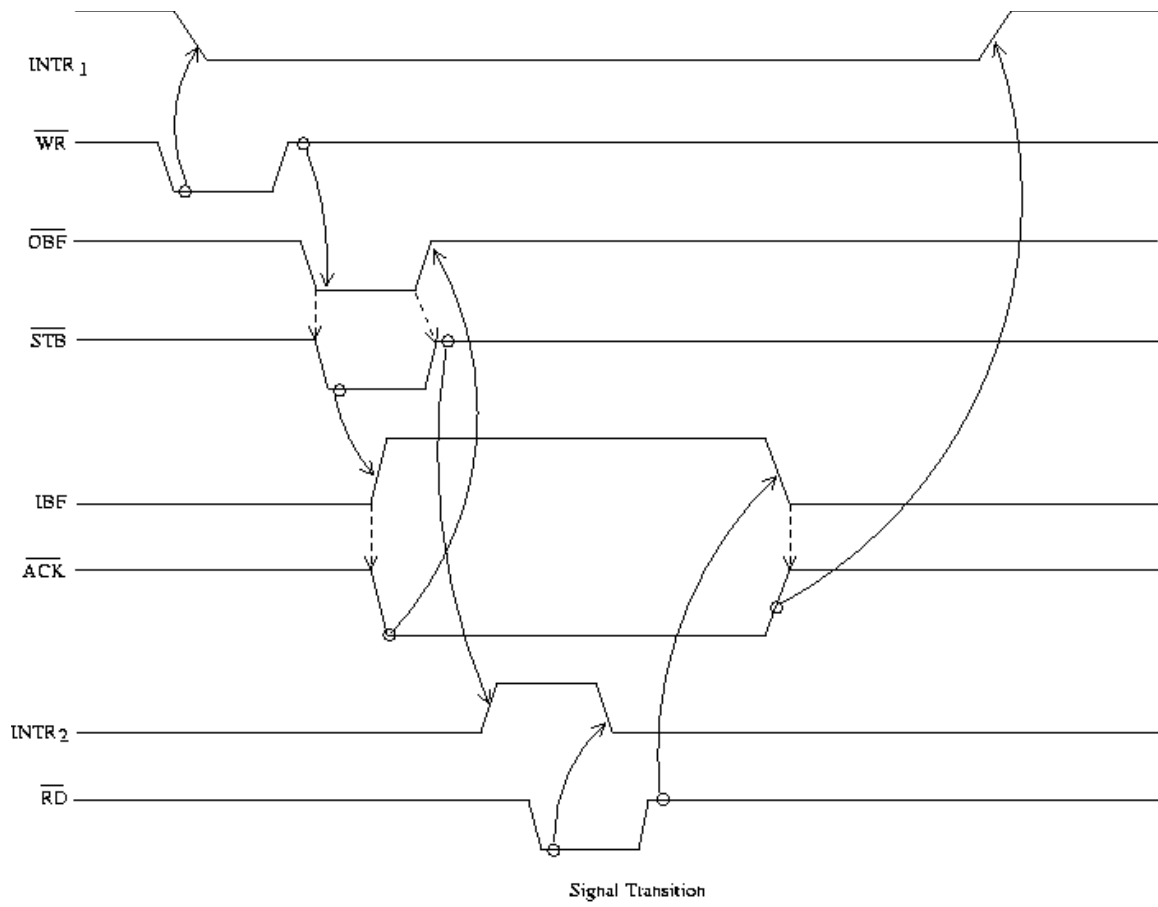
#### SEQUENCE

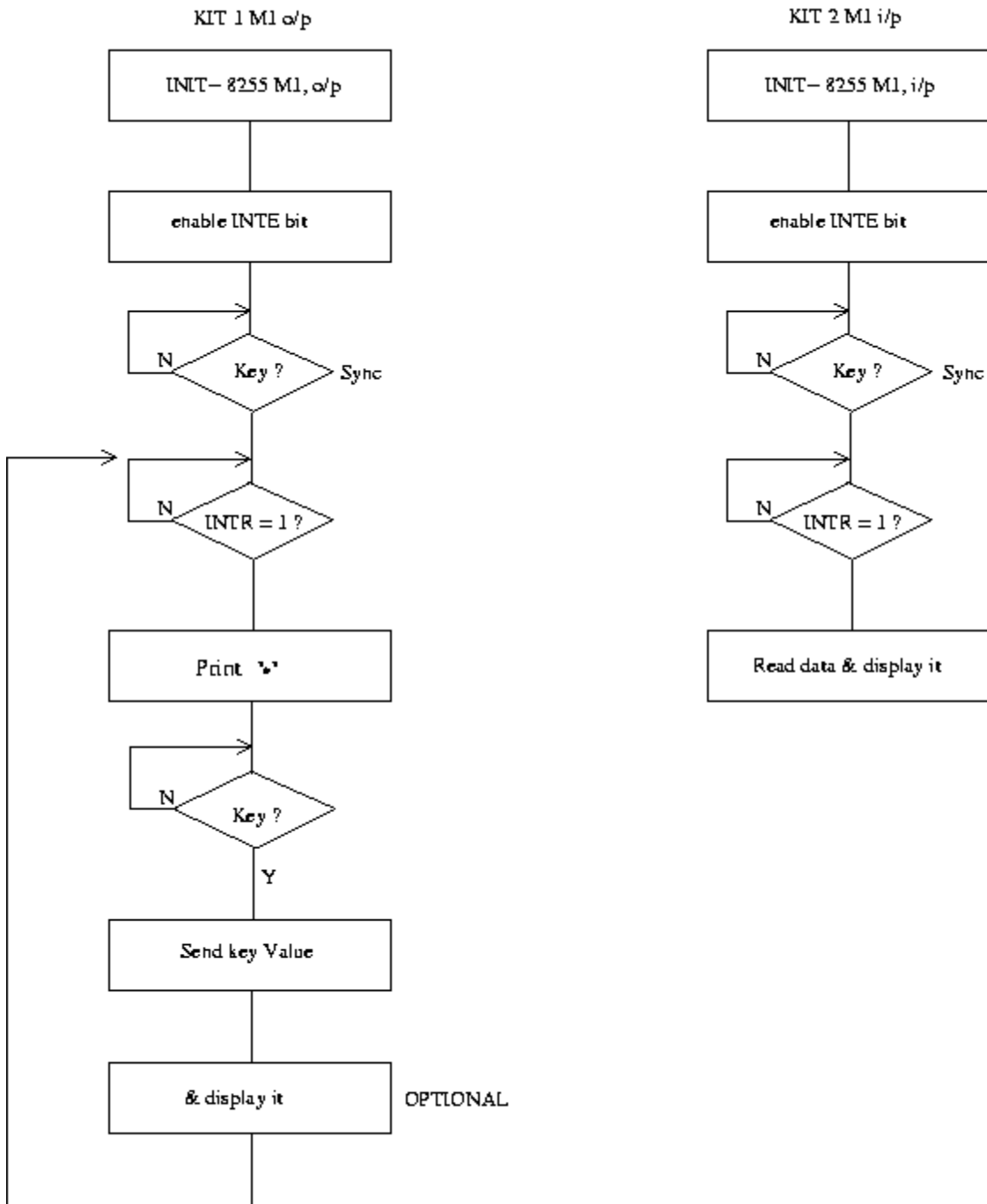
1. Terminal power on - DTR
2. Modem power on - DSR
3. Modem dials up remote computer
4. If computer is available, it will send back a specified tone - Link established
5. Terminals wants to send a character - RTS.
6. Modem Asserts CD.
7. When modem is ready to transmit - CTS.
8. Terminal sends character serially and Modem transmits.
9. Transmission over - Terminal makes RTS high.
10. Modem makes CTS high and Stops transmission.



3. It is desired to transfer data from kit1 to kit2 through the 8255's present on the kit. Show the interconnections between the kits and signal transition (starting from write on kit1 and ending with read on kit2, including interrupts and all other handshake signals) if 8255 on kit1 is programmed in mode1 output and 8255 on kit2 in mode1 input. Give flow chart for transmitting data through the keyboard on kit1, and for receiving data on kit2. Make appropriate assumptions wherever required. [10]



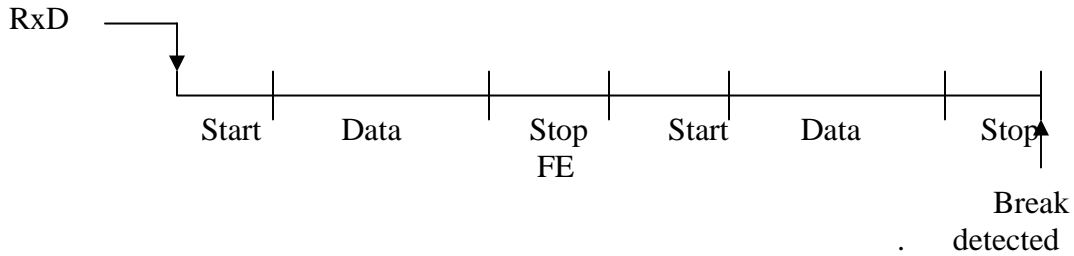




FLOW CHARTS

4. Explain in brief

- a. when is break condition detected in 8251 receiver.  
A break is detected at the receiver when it sees the line (RxD pin) low for two consecutive characters.



b. Use of x1 baud rate mode in 8251 when used in asynchronous mode.

X1 baud rate is used in Asynchronous mode for doing loop back testing (local as well as Remote) this makes the loopback test faster and works at  $TxC$  &  $RxC$  are the same in the case of loopback.

c. Hunt mode when 8251 is programmed in synchronous mode.

Hunt mode is used by the data receiving programme in Sync. Mode, this is done to detect sync. Characters, here the Receiver checks for sync character after every bit is strobed in. The USART comes out of hunt mode once the sync is detected..

d. Need for 2 character sync. When 8251 is programmed in synchronous mode.

2 character sync allows all combination of data to be transmitted (in 1 character sync the sync charc cannot be transmitted as data).

In 2 character sync, if the sync sequence appears in the data stream to be transmitted then the input stream is broken and the sync sequence is inserted.

Ex: Let 02, 03 be the 2 sync character, and if this appears in the data stream then we modify it as ... 02 02 03 03

DATA SYNC SEQ DATA

e. Special fully nested mode in 8259.

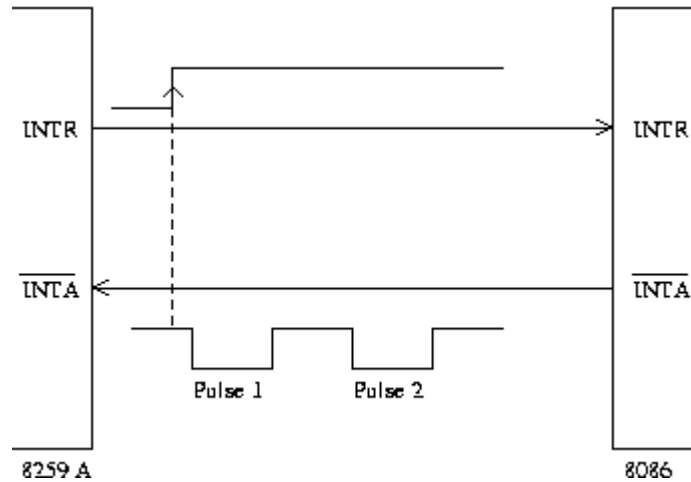
Special fully nested mode is for the MASTER 8259 when we have one or more slave 8259's connected to it. (CASCADE MODE CONNECTION).

In a fully nested mode the 8259 after acknowledging an Interrupt from level 'n', disables all Interrupts from level 'n' and below.

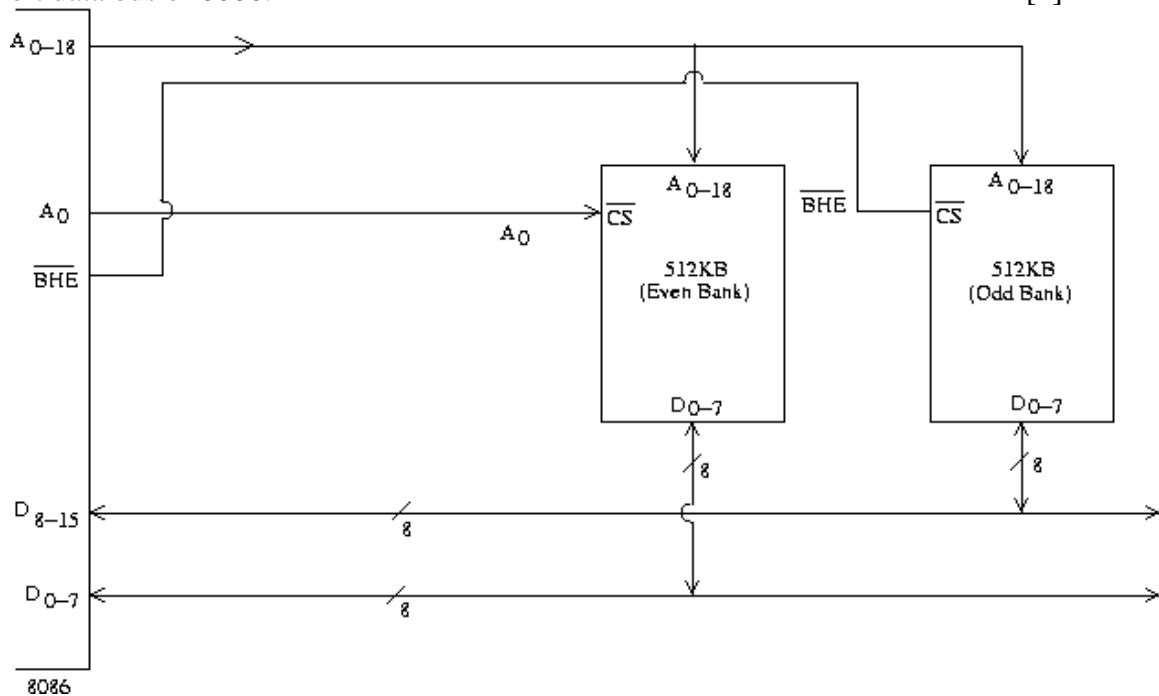
Whereas when programmed in special fully nested mode (CASCADE Connection), it allows Interrupts from the same level in case of a slave connected at the Interrupt level, and disables all Interrupts below this level.

f. How 8259 works(INTR and /INTA behavior) when it is connected to 8086.

In response to INTR going high, 8086 (if interrupts are enabled and INTR is the highest Interrupt pending) acknowledges the INTR with INTA pulses nothing happens at the first INTA pulse (if 8259's are connected in cascade, then at the end of 1<sup>st</sup> INTA pulse the Master 8259 floats the slave address (if required), and then during the second INTA pulse the selected 8259 (Master or slave will respond with a vector Byte nn (00-FF). This is interpreted as INT nn by 8086, and it executes the ISR for INT nn by getting the CS:IP for this INT from the Interrupt Vector Table (IVT).



5. With the help of a neat diagram show how 1MB of memory is interfaced to the 16 bit data bus of 8086. [4]



8086 knows from the Instruction, when it is reading a Byte or a word, it also knows the address (even or odd) from where it is reading and so it generates BHE appropriately i.e.

OPERATION	$\overline{\text{BHE}}$	$A_0$
Byte from EVEN A.	1	0
Byte from ODD A.	0	1
Word from ODD A	0	0
Word from ODD A	0	1 ← 1 <sup>st</sup> read one byte
	1	0 ← then the 2 <sup>nd</sup> byte

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1. What is the need for using a Schmitt trigger receiver at the reset input from the push-button to generate the reset pulse to the system. [2]
  - To reset the system reliably, reset signal should be active for a specified period. Once manual reset is done, reset will be low for few milli seconds which is sufficient to reliably reset the entire system. As the capacitor charges and reaches just the voltage corresponding to 1, if any, noise is picked up by the signal, it may fluctuate and may give reset for a short duration. As the reset has reached 1 a clock might have started. Under these conditions of clock presence and unreliable reset signals, things might go haywire. If you place a Schmitt trigger then due to hysteresis, noise on the reset line may not affect the reset signal as it might not have crossed the threshold level. This gives the system a reliable operation. Hence Schmitt trigger is highly desirable.
  
2. Connect a 27 pin SRAM organized 8K x 8 to 8085 processor and write a programme to check the memory by writing 0's in all locations and checking them by reading and followed by writing all 1's and checking the same in all locations. Give a neat circuit diagram and the programme. If the checking is successful, put on a green LED and if it is unsuccessful put on a red LED. [5]
  - Program
    - Initialize all LEDs
    - Store all Zero's to RAM
    - Start reading from RAM
      - If not Zero anywhere
      - Jump to Error Routine
    - Store all 1's to RAM
    - Start Reading from RAM
      - If not One anywhere
      - Jump to error routine
    - Glow green LED
    - Error Routine
      - Glow Red LED
    - Halt
  
3. Explain :
  - a) Two architectural differences between 8085 and 8086
    - 8085 is an 8-bit processor whereas 8086 is a 16 bit processor. In 8085 the fetch execute of machine instructions are sequential whereas in 8086, they are overlapped.
    - One feature introduced in 8086 which was not there in 8085 is segmentation to have multiprogramming facility.
    - 8086 has Floating point and I/O Processor support through 8087 & 8089.

- b) Why reset need to be given to 8255.
- Essentially to make all the ports to act as inputs so that there won't be any clash of signals on this line.
- c) Main Architectural difference between 8088 and 80188.
- 8088 is a microprocessor whereas 80188 has other units in it and can be classified as a microcontroller.

[3]

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