P.C.I. Express

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Introduction

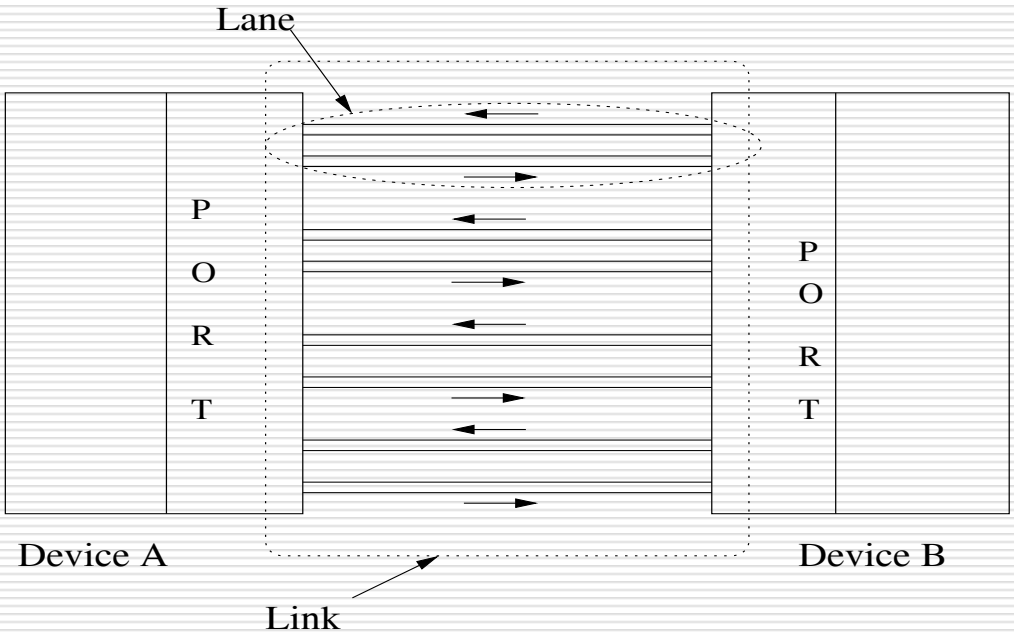
- High speed, serial pathway.
- Dual – unidirectional paths.
- Bandwidth of 2.5 Gigabits per second per direction.

Benefits of PCI Express

- Layered Architecture.
- Compare maximum theoritical bandwidths.
  - PCI : 32-bit bus at 33 MHz , 132 MB/sec
  - PCI-X : 64-bit bus at 66.66 MHz , 533 MB/sec
  - PCI Express : Bandwidth of 2.5 Gigabits per second per direction and potential for growth to 10 Gigabits/sec/direction.
- Point-to-Point Interconnect.

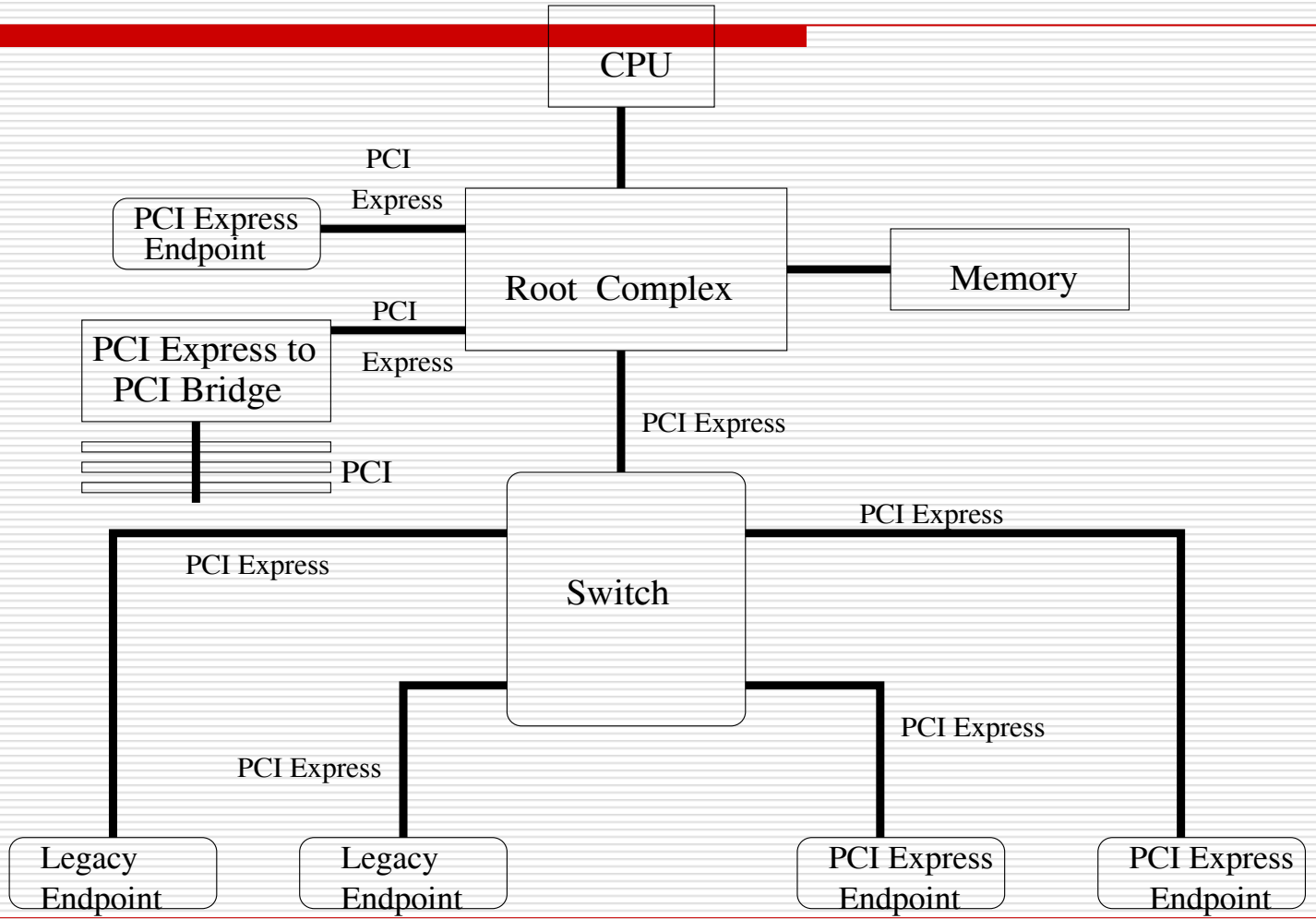
PCI Express Architecture Overview

- Links and Lanes.
- *Serial links : x1 , x2 , x4 , x8 , x12 , x16 and x32.*



- PCI Express Device Types
  - Root Complex
  - PCI Express to PCI Bridge
  - Endpoint
  - Switch
- PCI Express Transactions
  - *Request and Completion*
  - *Requester* and *Completer*

PCI Express System Architecture



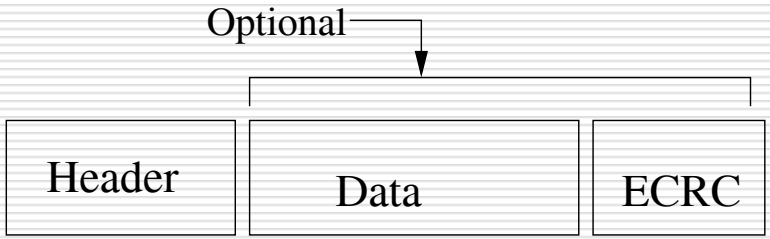
Transaction Types

- Memory Transactions
- I/O Transactions
- Configuration Transactions
- Message Transactions

Architectural Build Layers

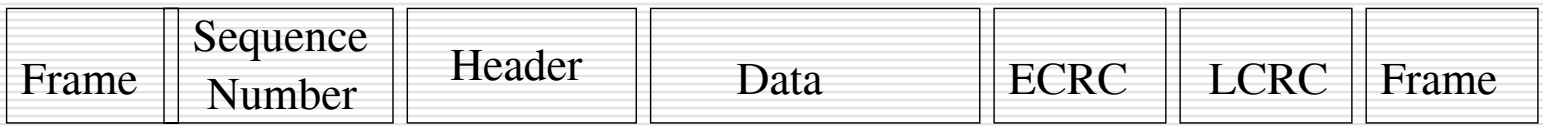
- Transaction Layer
- Data Link Layer
- Physical Layer

Transaction Buildup through Architectural Layers

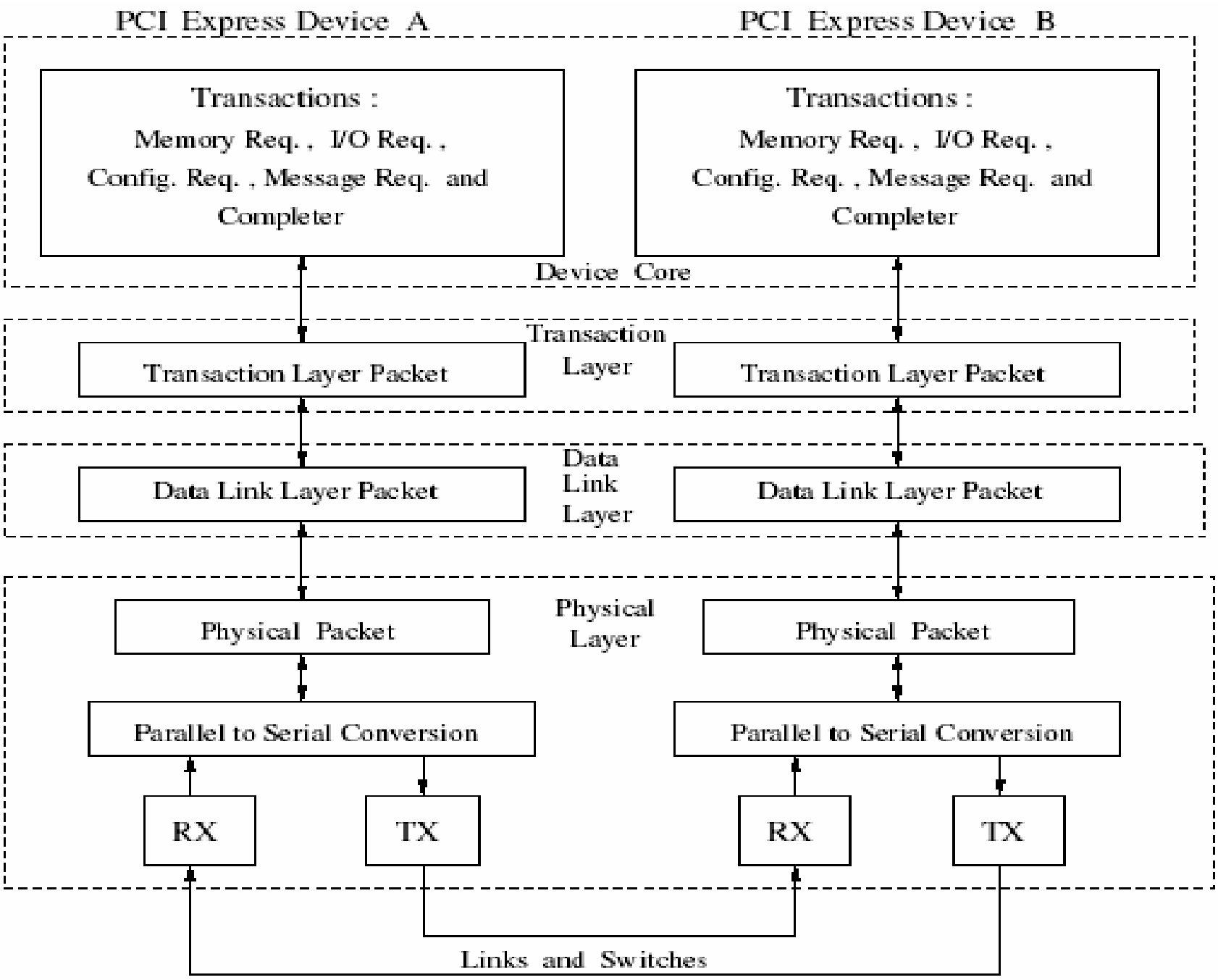


At Transaction Layer

At Data Link Layer



At Physical Layer


PCI Express Device A
PCI Express Device B
Transactions :
Memory Req. , I/O Req. ,
Config. Req. , Message Req. and
Completer
Transactions :
Memory Req. , I/O Req. ,
Config. Req. , Message Req. and
Completer
Device Core
Transaction
Layer
Transaction Layer Packet
Transaction Layer Packet
Data
Link
Layer
Data Link Layer Packet
Data Link Layer Packet
Physical
Layer
Physical Packet
Physical Packet
Parallel to Serial Conversion
Parallel to Serial Conversion
RX
TX
RX
TX
Links and Switches

Transaction Layer Architecture

- Create PCI Express request and completion transactions.
- Both *Transmit* and *Receive* Functions.
- Receives request data from *Device Core.*
- Receives incoming transactions from *Data Link Layer*.
- Uses Transaction Layer Packets for communication.

Transaction Layer Packet (TLP)

- *Request* and *Completion* Information is communicated.
- Transaction Layer
  - Generates outgoing TLPs.
  - Accepts incoming TLPs.
- Transaction Layer Packet consists of
  - *Header*
  - *Data payload*
  - *TLP Digest* or *ECRC*

Data Link Layer Architecture

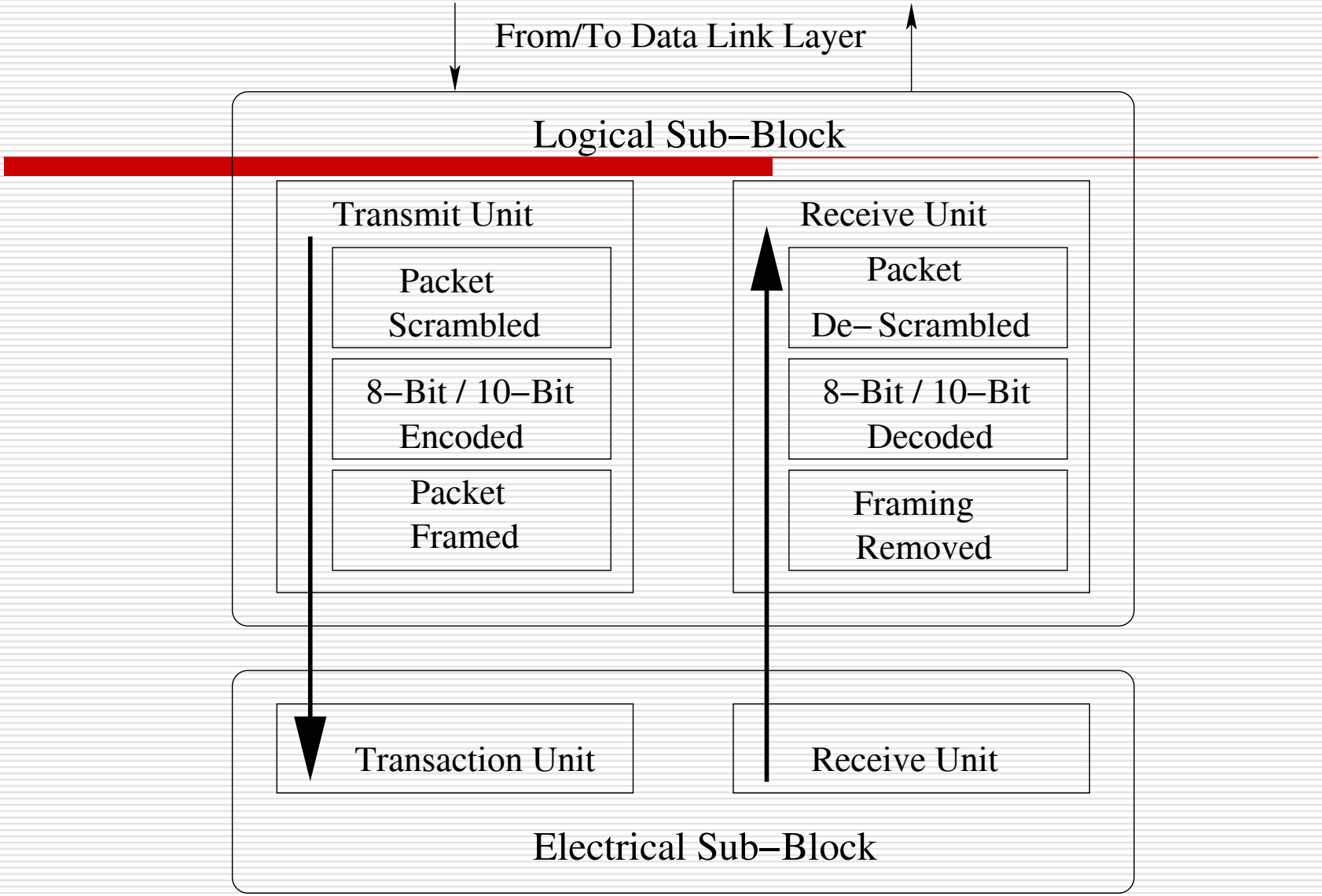
- Serves as *gatekeeper* for each individual link.
- Ensures that each packet makes it across the link.
- Takes TLPs from the transmit side of the Transaction Layer.
- Adds a *sequence number* and an *LCRC*.
- Accepts the packets from Physical Layer.
- Checks the sequence number and LCRC.

Data Link Layer Packet (DLLP)

- Originate at the Data Link Layer.
- Intended for the Device on the other side of link.
- DLLPs are of four types :
  - Ack DLLP
  - Nak DLLP
  - FC DLLPs
  - PM DLLPs

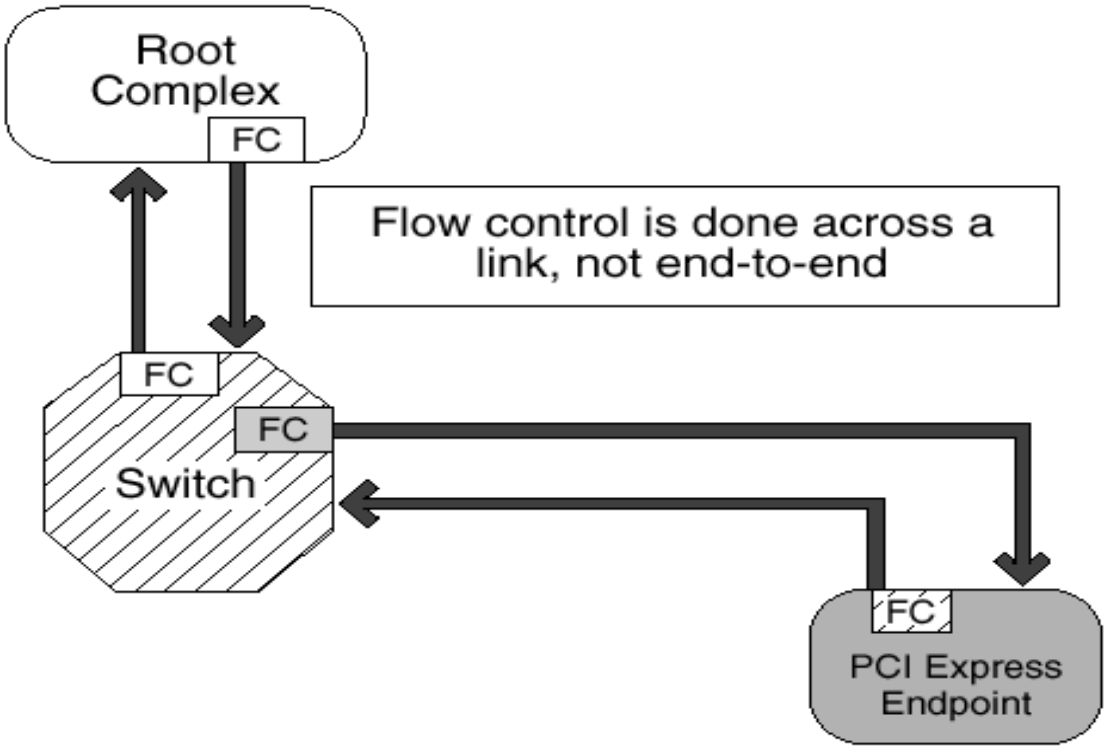
Physical Layer Architecture

- Sub-blocks of Physical Layer :
  - ❖ Logical Sub-block
  - ❖ Electrical Sub-block
- Logical sub-block has *separate* *Transmit* Unit and *Receive* Unit.
- Electrical sub-block has separate *Transmit* and *Receive* buffers.


From/To Data Link Layer
Logical Sub–Block
Transmit Unit
Packet Scrambled
8–Bit / 10–Bit Encoded
Packet Framed
Receive Unit
Packet De– Scrambled
8–Bit / 10–Bit Decoded
Framing Removed
Transaction Unit
Receive Unit
Electrical Sub–Block

Flow Control

- To prevent receiver buffer overflow.
- Local to each link.



- Virtual Channels.
- Traffic Classes.
- Each VC has its own set of queues and buffers and control logic.
- Supports 8 different Traffic Classes.
- Flow Control Rules.
  - PCI works as *Single Lane Bridge*.
  - PCI Express Flow Control Model works as *Highway with four lanes* in both directions.

- Flow Control at the Transmitter.
  - Credits-Consumed
  - Credits-Limit
- Flow Control at the Receiver.
  - Credits-Allocated
  - Credits-Received
- An Example of Flow Control Credits.
  - B indicates 4 PH Credits and 40 PD Credits.
  - A sends 2 requests, 1 PH + 10 PD units each.
  - Wants to send another request that uses 1 PH and 30 PD credits.

Thank you .