VLSI

Overview

Basic features of VLSI are :

- Chip is a thin silicon surface (2-dimensional)
- Same material is used for the wires and devices
- Since photographic process is used in the fabrication the resolution is limited to the wavelength and,therefore-
  Basic device size $\geq wavelength$
  $Wirelength \geq wavelength$
  $Separationbetweendistinctcomponents \geq wavelength$

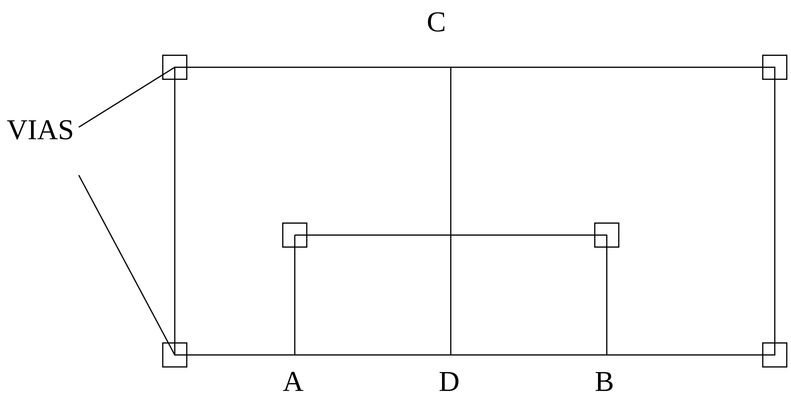
With the improvement in the technology,the only change in the chip design is that of the reduction of the wavelength.

Thompson Grid Model

Is a model of the VLSI design, having the following features -

- Chip:Rectangular area with evenly spaced vertical and horizontal tracks.
- Processors are placed at track intersections.
- Wires occupy tracks.
- "Via" used to connect horizontal and vertical tracks.
- Systolic operation : Signals propagate in one clock tick across wires independent of the length.

Example-



A,B,C,D-PROCESSORS

The cost of such a model can be measured in terms of -

- **Bounding box area**
  for the above example the bounding box area equals -
  3 * 5 = 15 (in terms of the no of tracks).
- **Max. wire length**
  from A to C or B to C in the above example.
- **No. of Vias**
  06 in the above example.
- **No. of Crossings**

Such a model however has certain limitations,which can be catagorised as -

- Unit delay wires: This model assumes that signals travel throughout the length of the wire,in one clock,independent of the length of the wire.
  In reality : Delay = O(Log L) : for capacitive wires
  and = O(L) : for capacitive and resistive wires

- 2-Terminal wiring
  NO Buses
  K-terminal bus can be approximated using K leaf tree.

- Rectilinear wiring : The model allows only straight/horizontal tracks.Real chips have arbitrary shapes for the wires.

- Node limitations : This model allows for node deg. ≤ 4.
  However if greater degree is desired, allow the processor to occupy several grid points.

- This model has two layers of wiring whereas real chips may have 5-6 layers

Leema-

Let A= Area in K layer model
Then area in 2-layer grin model is
O (K^2) = O(A) —- if K = Constant
Idea

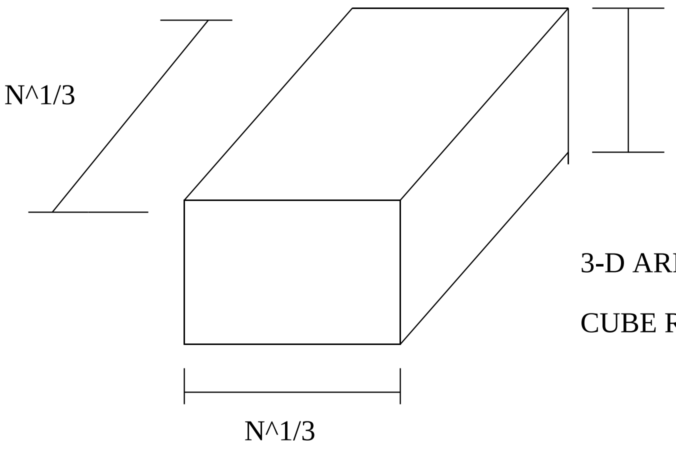
Stagger and project
First the model is expanded by a factor of K and then the layers are slided in a manner such that when they are collapsed on the lower layer, they are separated by a unit distance apart.

Example layouts-
2-D Array

$\sqrt{N} \times \sqrt{N}$ processors
Layout : Square of side $\sqrt{N}\}$
$Area = O(N)$
$Max.WireLength = O(1)$

3-D Array

$\sqrt[3]{N}) \ \times \sqrt[3]{N} \times \sqrt[3]{N}$ processors
Consider K= $\sqrt[3]{N}$ Layer Layout



3-D ARRAY OF

CUBE ROOT N-PROCESSORS

Area of K-layer model
A = O($\sqrt[3]{N} \times \sqrt[3]{N}$)

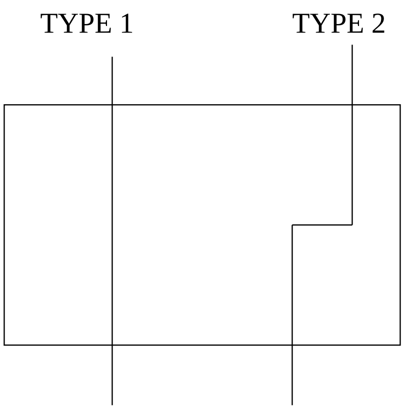
Area of two layer model
A = O(K$^2.A$)
$= O(\sqrt[3]{N}^2 \times \sqrt[3]{N}) \times \sqrt[3]{N})$

Having seen the layouts of the common networks we now discuss the lower bounds on the layout area-

Theorem-

For graphs with bisection width B , layout area = ω (B^2)

TWO TYPES OF CUTS



There exists a cut of type 1 or of type 2 such that the
no. of nodes to the left is $\leq$ N / 2
no. of nodes to the right is $\leq 4N/2$

This is proved by the sliding cut argument.
Proof-
Due to type 1 cut , the no. of wires crossing the cut $\geq$ B
Due to type 2 cut, the no. of wires crossing the cut $\leq$ h+1
Therefore-
B $\leq$ h+1
B / 2 $\leq$ h
Implies That-
$B^2/4 \leq h^2 \leq A$

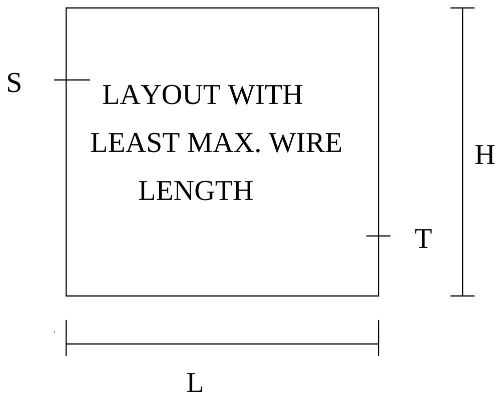
Next, we discuss the lower bounds on the wire length-

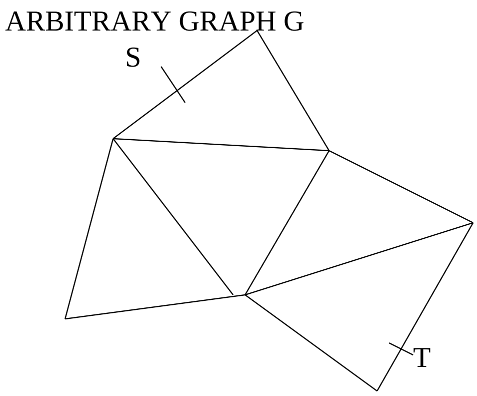
Theorem-

Let A = layout area

d = diameter

Then the maximum wire length = $\omega(\sqrt{A}\ \ d)$





S and T are the active elements on the left and right boundary of the chip, respectively.

s,t are the pre-images of S,T in the graph G.

P: shortest path from s to t in G.

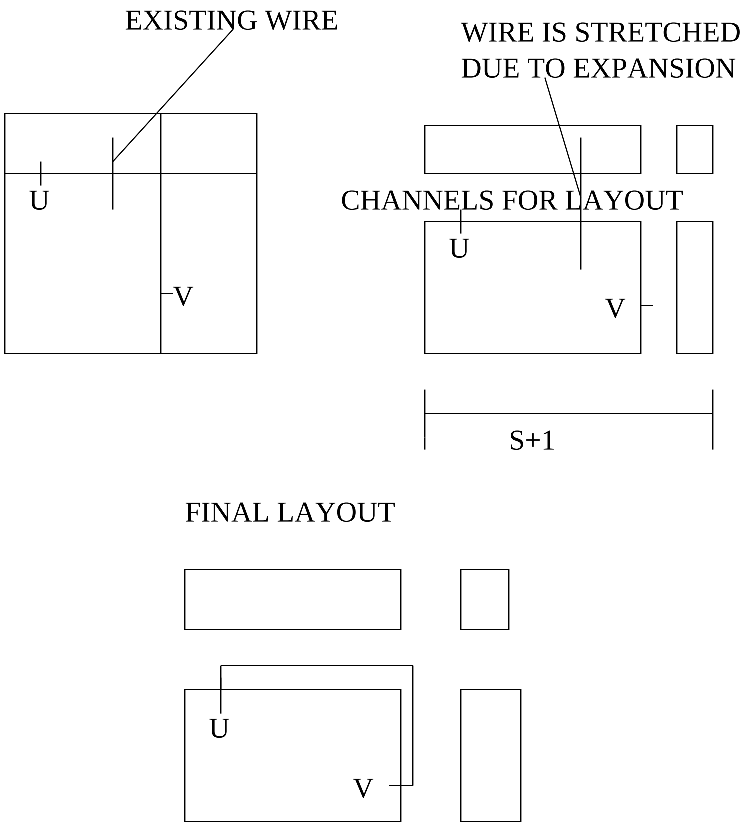
In the layout P $\geq$ l

In the graph G, no. of edges in P $\leq$ d+2

Therefore some edge has length $\geq$ l / (d+2) $\geq$ $\sqrt{A}$ / 2d

Slicing

Is a technique for adding a vertex (i.e. processor) or an edge between vertices.Adding of a vertex may in the worst case increase the side length by O(1).This wil happen only empty intersection (say for the mesh) available for the placing of the new vertex.
In case of an edge to be added,the layout may have to be expanded horizontally as well as vertically.Any wire crossing the expansion slot may have to be stretched in this case (ref figure below).
Also,laying of an edge may turn out to be more complicated if any specific orientation is required.



Divide and conquer layouts

This technique divides the graph into subgraphs,with no interconnecting edges between them, and creates a layout for these individual subgraphs and then does the interconnections using the sliding technique.

Vertex bisector

A N-node graph G=(V,E) has f(N) node bisector if V can be partitioned into A,B,and S, such that

- $|$ A $|$, $|$ B $|$ $\leq$ N / 2

  $|$ S $|$ $\leq$ f(N), and

- No edges are present fron A to B

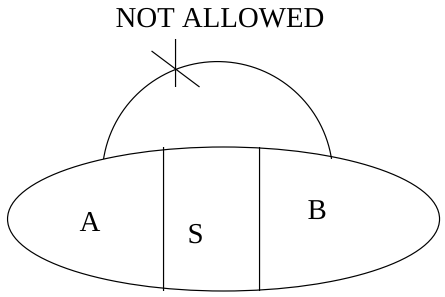
Examples-

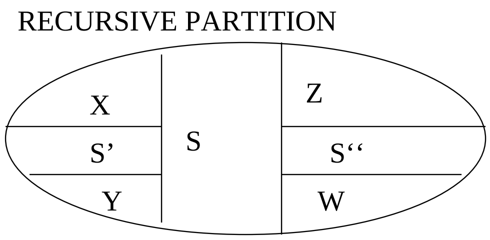
- CBT - f(N) = 1
- Mesh - f(N) = $\sqrt{N}$
- Butterfly - f(N) = N / logN

If the bisector property holds recursively-

- bisect G giving A,B,and S.
- bisect A giving X,Y, and S'
- bisect B giving Z,W, and S"

For the final layout -





Insert the nodes ($S \cup S` \cup S``$) and edges into the layout using **slicing**.
The side length is therefore -
S(N) = 2S (N / 4) + f(N) α + 2f(N/2) β

Layout of Planer Graphs

Theorem
Any N node,bounded degree planer graph can be layed out in area = O(N (log)$^2 N$)

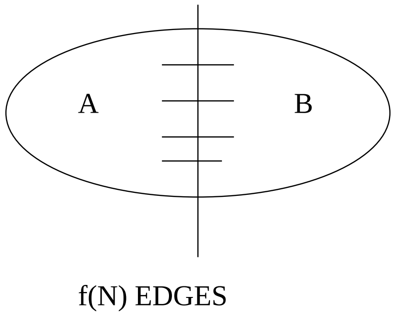
$Proof -$
$PlanerGraphhasO(\sqrt{N})$ bisectors
Remove $\sqrt{N}$ vertices to break the graph in two parts with N/2 vertices.

S(N) = 2S(N/4) + $\sqrt{N}$ + 2 ($\sqrt{N}$/2)
= 2S(N/4) + O ($\sqrt{N}$)

Computing it recursively, we get
S(N) = $\sqrt{N}$ log N

Remarks

- Edge bisectors are also useful.



$$S(N) = 2S(N/4) + f(N) + 2f(N/2)$$

- Precise recurrence might be sharper, e.g. butterfly.
- Useful for many networks.

Layouts of General Graphs
Theorem

Any N node,degree d graph can be layed out in area $O((N)^2(d)^2)$

Proof