

Memory Management in SPARC

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Memory Management in SPARC: Overview

- **SPARC** (*Scalable Processor ARChitecture*): a third generation, 64-bit processor.
- Supports software Translation Lookaside Buffers (TLBs) and Multiple Page Sizes.
- Provides separate Instruction and Data MMUs
- In addition, has a second level cache for Translation Table in the memory called Translation Storage Buffer..

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MMU in SPARC

- Virtual Address Translation
 - OS translates 64-bits virtual address space into 44-bits virtual address space.
 - MMU translates 44-bits virtual address space to 41-bits physical address space.
- Translation Table Entry
- Translation Storage Buffer
- Data Translation Lookaside Buffer
- Instruction Translation Lookaside Buffer

Translation Table Entry

- Stores information for a single page mapping.
- Consists of 2 64-bit words: **Tag** and **Data**

Translation Storage Buffer

- Acts as a cache of Software Translation Table to reload the TLB on a miss.
- MMU provides precomputed pointers for 8kb and 64kb pages in TTE.
- n lsb of the respective virtual page number (VPN) are used as offset from TSB base address. = $\log_2(\text{no of TTE in TSB})$.

Translation Lookaside Buffers

- **TLBs in D-MMU**

- Contains 2 TLBs: each 512-entry two way associative.
- Each TLB can be programmed for any of the 4 page sizes.
- Works as 1024-entry TLB if both programmed for the same page size.

- **TLB in I-MMU**

- Contains 128-entry, 2 way associative exclusively for 8kb unlocked page translations.
- Contains 16-entry full associative TLB for larger page translations and locked pages for all sizes.

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