Memory Management Unit for the Intel Family of processors

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1 Introduction

- What is MMU?
- Solves Fragmentation Problem
- TLB - Translation Lookahead Buffer
- Instruction MMU and Data MMU

2 TLB - Translation Lookahead Buffer

- Mapping from virtual address to physical address

- Independent enabling of instruction translation and protection

- Page-level access control using the translation mechanism

- Storage attributes for cache policy and speculative memory access control

3 MMU Example - Intel(R) Processors

- Instruction Memory Management Unit: Provides protection information to regions of the instruction memory and facilitates cache management.

- Data Memory Management Unit:Provides protection information to regions of the data memory and facilitates cache management.

- Intel 80200 : 32-Entry Instruction Memory Management Unit Enables logical-to-physical address translation, access permissions, I-Cache attributes.

- Intel 80200 : 32-Entry Data Memory Management Unit Enables logical-to-physical address translation, access permissions, D-Cache attributes.

- Integrated MMU - Support for virtual memory and demand paging.

- Intel486 : Capability to address up to 4 gigabytes of physical memory and 64 terabytes of virtual memory.

4 References

- www.intel.com
- www.linux-mag.com
- www.xilinx.com