

Lab-9 (Musical notes generation)

Introduction

The Atyls board includes a National Semiconductor LM4550 AC '97 audio codec (IC3) with four 1/8" audio jacks for line-out (J5), headphone-out (J7), line-in (J4), and microphone-in (J6). Audio data at up to 18 bits and 48KHz sampling is supported, and the audio in (record) and audio out (playback) sampling rates can be different. Following signals represent the interface signals to AC '97 audio codec to FPGA as shown in figure-1.

<u>Signal Name</u>	<u>FPGA Pin</u>	<u>Pin Function</u>
AUD-BIT-CLK	L13	12.288MHZ serial clock output, driven at one-half the frequency of the 24.576MHz crystal input (XTL_IN).
AUD-SDI	T18	Serial Data In (to the FPGA) from the codec. SDI data consists of AC '97 Link Input frames that contain both configuration and PCM audio data. SDI data is driven on the rising edge of AUD-BIT-CLK.
AUD-SDO	N16	Serial Data Out (to the codec) from the FPGA. SDO data consists of AC '97 Link Output frames that contain both configuration and DAC audio data. SDO is sampled by the LM4550 on the falling edge of AUD-BIT-CLK.
AUD-SYNC	U17	AC Link frame marker and Warm Reset. SYNC (input to the codec) defines AC Link frame boundaries. Each frame lasts 256 periods of AUD-BIT-CLK. SYNC is normally a 48kHz positive pulse with a duty cycle of 6.25% (16/256). SYNC is sampled on the rising edge of AUD-BIT-CLK, and the codec takes the first positive sample of SYNC as defining the start of a new AC Link frame. If a subsequent SYNC pulse occurs within 255 AUD-BIT-CLK periods of the frame start it will be ignored. SYNC is also used as an active high input to perform an (asynchronous) Warm Reset. Warm Reset is used to clear a power-down state on the codec AC Link interface.
AUD-RESET	T17	Cold Reset. This active low signal causes a hardware reset which returns the control registers and all internal circuits to their default conditions. RESET must be used to initialize the LM4550 after Power On when the supplies have stabilized. RESET also clears the codec from both ATE and Vendor test modes. In addition, while active, it switches the PC_BEEP mono input directly to both channels of the LINE_OUT stereo output.

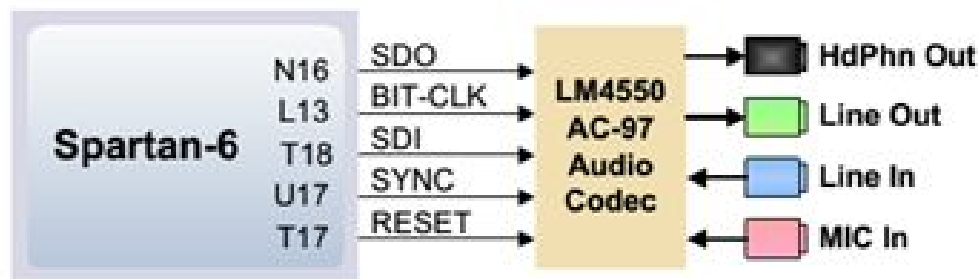


Figure 1 Interface between audio codec and FPGA

Sample Code Overview

Figure-2 shows the main components and their interface in the sample code

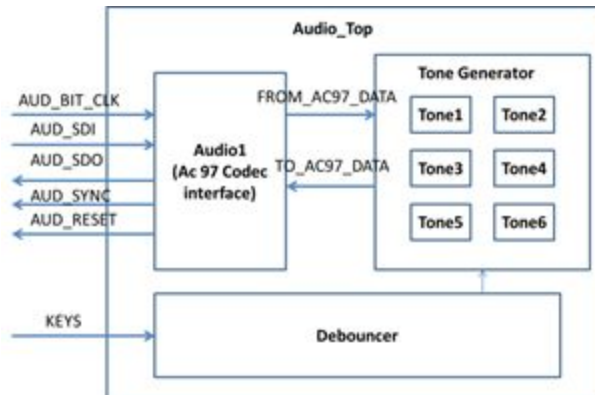


Figure 2 Main components in sample code and their interface

In the sample code, we have considered sample rate at 48khz. Sample code has only one component inside the *tone generator* module which generate tone at 750Hz. *Tone750Hz* module has 64 (48khz/750) samples of 20-bit Pulse coded modulation (PCM) data. 64 samples are taken by sampling one complete cycle of sine-wave of frequency 750Hz at periodic interval.

How it works? (Simple Overview)

When you press key on the board assigned for tone generation, it will take the PCM data stored in the *Tone750Hz* module and pass it to the *Ac97 codec interface* module. Interface module forwards this data to codec h/w present on board. Codec convert this digital data into analog data using ADC (analog to digital converter). After converting to analog data codec output this data to the *Line out*.

Table 1 Tone and frequency

Tone1	523.251 Hz
Tone2	587.33 Hz
Tone3	659.255 Hz
Tone4	698.456 Hz
Tone5	783.991 Hz
Tone6	880 Hz
Tone7	987.767 Hz

Things to be done in lab

In this lab you need to replace *tone750Hz* module with 7 different modules (tone1, tone2,...,tone7) where frequency of each tone is given in the table-1. We have provided you PCM data in Hex format for each frequency use it to create 7 *tone* modules similar to *tone750Hz* module. You will have 7 keys (push button/up-down) as input, where each key is assigned for a different tone. Each key input is passed through a *debouncer* module and

output of *debouncer* module is given to the *Tone generation* module. Based on a key which is in *high* state (pressed), *tone generator* module will give PCM data from respective *Tone* module as output to *To_ac97_data* line. If multiple keys are pressed simultaneously, give priority to higher frequency tone.