CS226 Practice Problem Set 6 (Spring 2016)

Date posted: April 11, 2016   **Expected Solving Time: 1 hour**

- *Be brief, complete and stick to what has been asked.*

- *Unless asked for explicitly, you may cite results/proofs covered in class without reproducing them.*

- *If you need to make any assumptions, state them clearly.*

- ***The problems/sub-problems marked ⋆ are "must-solve" problems, i.e., you are required to submit solutions of these problems through moodle. The remainder of the problems are for practice.***

- ***You are strongly encouraged to solve these on your own to ensure you understand the material being taught in class.***

- ***Mutual discussion on the non-⋆ problems is allowed. Please try to solve the ⋆ problems on your own. Please read the guidelines on the course webpage if you don't understand the distinction between the two.***

1. We have seen in class that different input-to-output paths in a circuit may have different delays, and this can cause a single transition on an input to cause multiple transitions on the output. In this problem, we'll be concerned with this phenomenon.

   Consider the circuit shown in Fig. 1. The numbers within the gates denote their input-to-output delays, and are assumed to be constant.

   $(a^\star)$ We wish to make the inputs of the circuit transition as follows:

   - Transition T1: $abcd = 0010$ to $abcd = 0011$
   - Transition T2: $abcd = 0011$ to $abcd = 0111$
   - Transition T3: $abcd = 0111$ to $abcd = 0110$
   - Transition T4: $abcd = 0110$ to $abcd = 0010$

   Note that the value of the output F of the circuit for each of the input combinations before or after a transition is 1. Note also that in each of the transitions T1 through T4, only one of the inputs b and d changes. Assume further that in each case, the circuit is *stable* (i.e. no output or internal wire is changing or has a change pending on it) when the corresponding input changes. This is equivalent to assuming that the inputs of the circuit are held at their initial values for a very long time (greater than the maximum delay from any input to the output) before any input is changed.

   For each of the transitions T1 through T4, indicate the following:

   i. How many transitions occur at output F in response to the single input transition?

   ii. If the input transition occurs at time 0, what is the time of each transition (if any) at output F?

   iii. What are the paths through the circuit through which the input transition propagates to cause each of the transitions (if any) mentioned in the previous sub-question? You can indicate a path by writing a sequene of gate names from the input to the output, e.g. G1-G2-G3-G8.
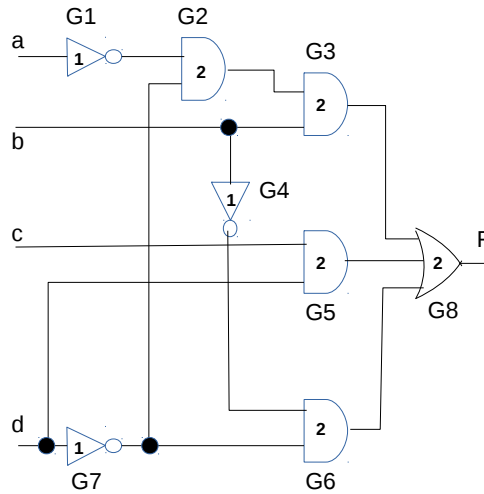
Figure 1: Circuit 1

(b) As you would have seen from your answer to the previous sub-question, some *glitches* or interme-diate transitions whose effects are nullified by subsequent transitions, may occur at the output F in response to a single transition on an input. Such glitches or intermediate transitions are also called *hazards*, and are best avoided.

You are required to eliminate all glitches/hazards in response to transitions T1 through T4 of the previous sub-question, without changing the logic function implemented by F.

   i. Indicate how you would change the delays of gates in Fig. 1 to achieve this. You are not allowed to change the circuit, but can only change the delays of gates. If required, you can use different delays from different inputs of a gate to its output.

   ii. Indicate how you would change the circuit without changing the delays of inverters, 2-input AND gates and 2-input OR gates to achieve this. You are not allowed to use anything other than inverters, 2-input AND gates and 2-input OR gates in your new circuit.

$2^\star$. A digital logic designer needs to design a complex controller that must run at a clock frequency of 10 GHz (10×10^9 Hz). For designing the controller, the designer has a choice of using one of two types (T1 and T2) of flip-flops in a library. The designer must use only one type of flip-flop in the entire design – i.e. she can't use some flip-flops of type T1, and some others of type T2. The following parameters are known for the two types of flip-flops:

- Clock-to-Q delay (min-max): $5 - 40$ ps (T1) and $3 - 43$ ps (T2)
- Setup time: 13 ps (T1) and 5 ps (T2)
- Hold time: 11 ps (T1) and 2 ps (T2)

The clock skew for distributing the clock to all flip-flops is 20 ps.

The combinational logic of the controller must be implemented using only specially designed 2-input NAND gates (a universal logic gate). The delay of each special 2-input NAND gate is given to be 5 ps.

Indicate with justification which type(s) of flip-flop can the designer use for the controller design.

2. Consider the sequential circuit shown in Fig. 2, where shaded rectangles represent D-flip-flops. The numbers within the gates denote their input-to-output delays in ns, and are assumed to be constant. Assume also for the sake of simplicity that the skew in the distribution of clocks to various flip-flops is 0 ns. Assume further that setup, hold and clock-to-q delays of the flip-flops are also 0 ns each.
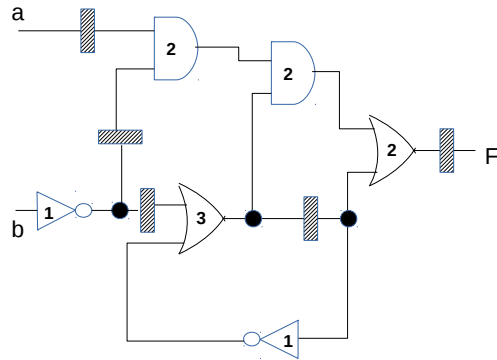

Figure 2: Circuit 2

We wish to use the technique of *re-timing* to reduce the minimum clock period or reduce the count of flip-flops, without changing the input-output behaviour of the circuit, and without changing the delays of gates in the circuit. Recall that re-timing involves moving flip-flops from the inputs to outputs of a gate, or from the output to the inputs of a gate.

(a) The minimum clock period of the sequential circuit in Fig. 2 can be seen to be 8 ns. Re-time this circuit and show the resulting circuit diagram such that the minimum clock period is reduced to 4 ns. What is the count of flip-flops used in your re-timed circuit?

(b) Re-time the circuit in Fig. 2 such that the count of flip-flops is reduced as much as possible. What is the minimum clock period and flip-flop count of your re-timed circuit?