CS226 Quiz 3 (Spring 2018)

Max marks: 20 **Time: 90 mins**

- *Be brief, complete and stick to what has been asked.*
- *Unless asked for explicitly, you may cite results/proofs covered in class without reproducing them.*
- *If you need to make any assumptions, state them clearly.*
- ***IIT Bombay prohibits the use of communication devices and internet enabled devices during examinations. You will be debarred from taking the examination if you are found accessing the internet during the examination.***
- ***Please do not engage in unfair or dishonest practices during the examination. Anybody found indulging in such practices will be referred to the D-ADAC.***

1. *[5+5 marks]* We wish to represent the following Boolean functions using ROBDDs with (possibly) complement edges and shared nodes.
   - $f_1 = (x_1 \oplus x_2) \cdot (x_3 \oplus x_4)$
   - $f_2 = (x_1 + x_2) \cdot (x_3 + x_4)$

   (a) Draw the shared ROBDDs with (possibly) complement edges and shared nodes using the variable order $x_1 < x_2 < x_3 < x_4$.

   (b) We now wish to implement the Boolean functions using 2-to-1 multiplexors and inverters, exactly as represented by the ROBDDs.

   Assuming the delay of from each input to the output of a 2-to-1 multiplexor is 10ns and the delay of an inverter is 4 ns, find the minimum and maximum delays from any of the inputs to any of the outputs in the above implementation of the Boolean functions.

2. *[10 marks]* Consider the coupled sequential circuits C_1 and C_2 shown in Fig. 1(a). The two circuits are fed by clocks Clk_1 and Clk_2 respectively, which are derived from a master Clk. The relation between Clk, Clk_1 and Clk_2 is given by the waverforms shown in Fig. 1(b).

   Note that outputs of C_1 are processed by combinational logic L_2 before being fed as inputs to C_2. Similarly, the outputs of C_2 are processed by combinational logic L_1 before being fed as inputs to C_1.

   Assume that the delays of all wires shown in Fig. 1(a) are 0. However, the logic blocks L_1, L_2, and the sequential circuits C_1, C_2 have gates and wires that have non-zero delays. All flip-flops in both C_1 and C_2 are assumed to be positive edge triggered, and both are assumed to start running together at a time instant corresponding to a common positive edge of Clk, Clk_1, Clk_2.

   Assume further that the circuit C_1 implements a state transition system that potentially changes the values of wires X_1 every 6^{th} rising edge of Clk_1 (starting from the first rising edge of Clk_1 as shown in Fig. 1(b)). Similarly, assume that the circuit C_2 implements a state transition system that potentially changes the values of wires X_2 every 4^{th} rising edge of Clk_2 (starting from the first rising edge of Clk_2 as shown in Fig. 1(b)). There are no changes in the values of X_1 or X_2 at other times.

   You are told that the clock skew within sequential circuit C_1 is s_1 and that within sequential circuit C_2 is s_2. Similarly, you are told that the setup and hold times of all flip-flops used in either circuit are a and b. The clock-to-q propagation delay of each flip-flop lies within c and d, where $c \leq d$. If the clock period of Clk is T, find the smallest and largest permissible delays through logic blocks L_1 and L_2.

   You may assume that s_1 and s_2 lie within the range $[T, 2T]$.

   Clearly show your reasoning for your answer.

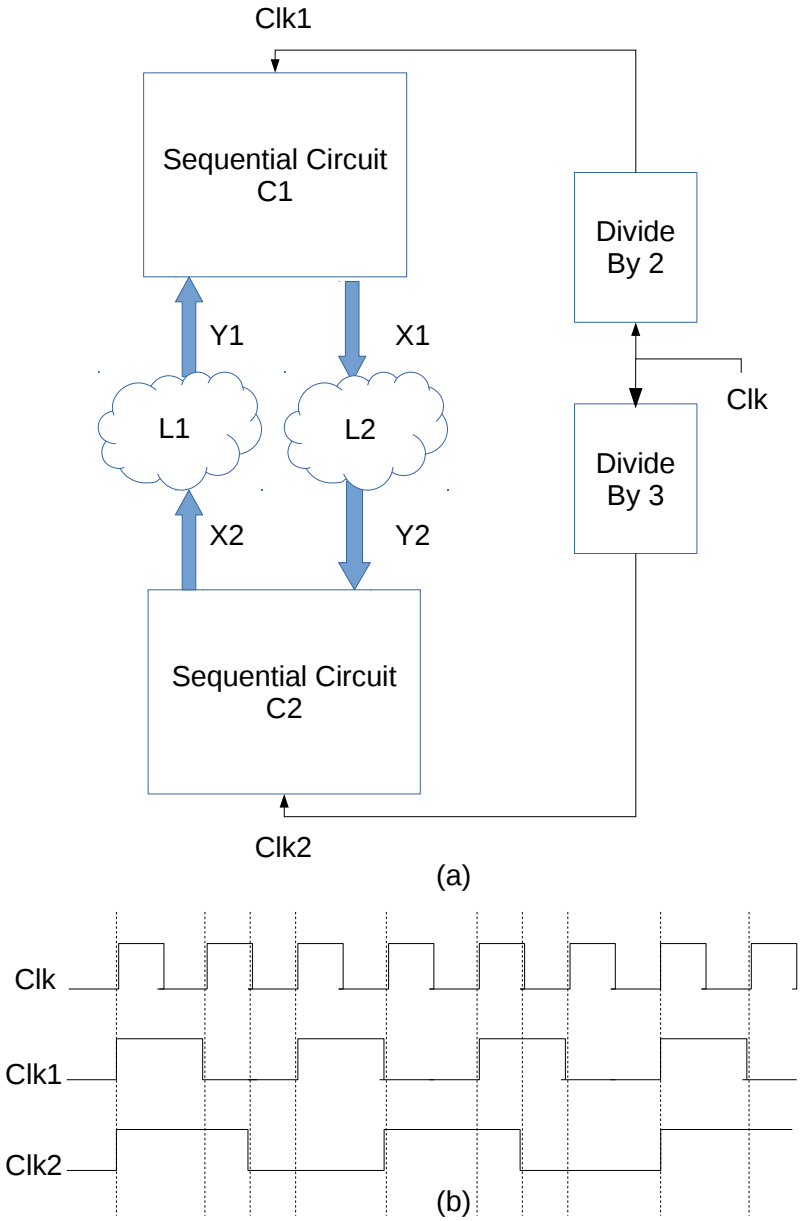

Figure 1: Circuit for Q2