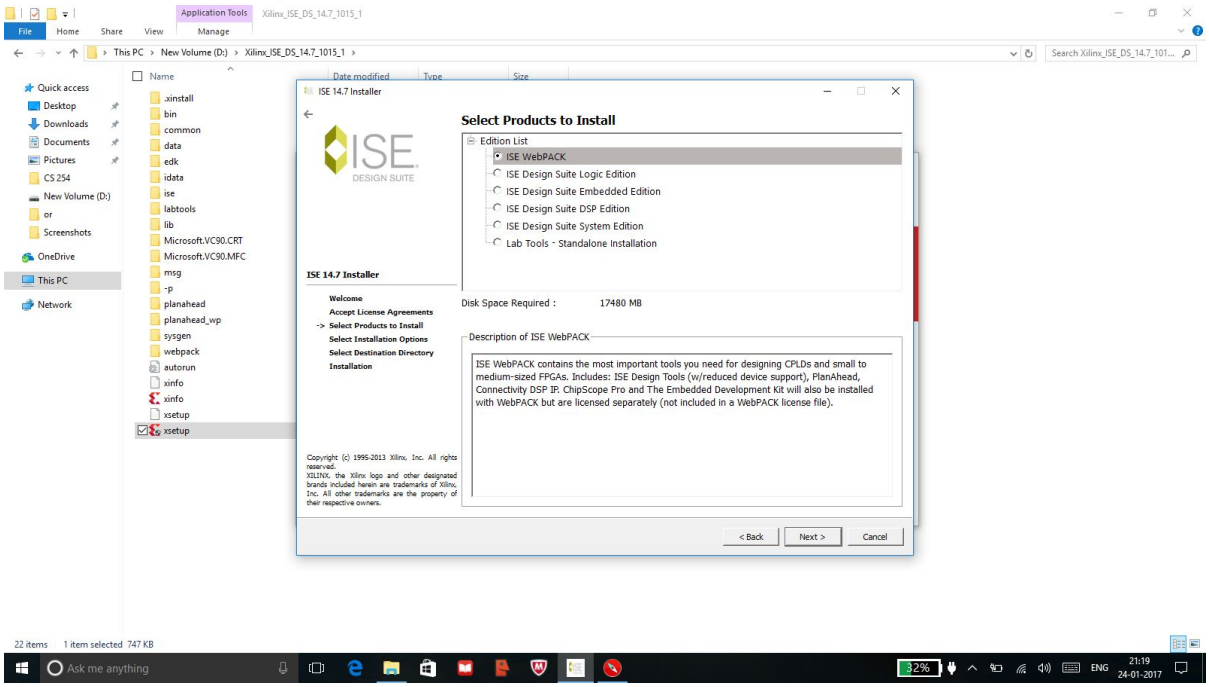
Installation

Download from http://10.130.4.2/cs254/Xilinx_ISE_DS_14.7_1015_1.tar

Ensure that you have enough space on the disk.

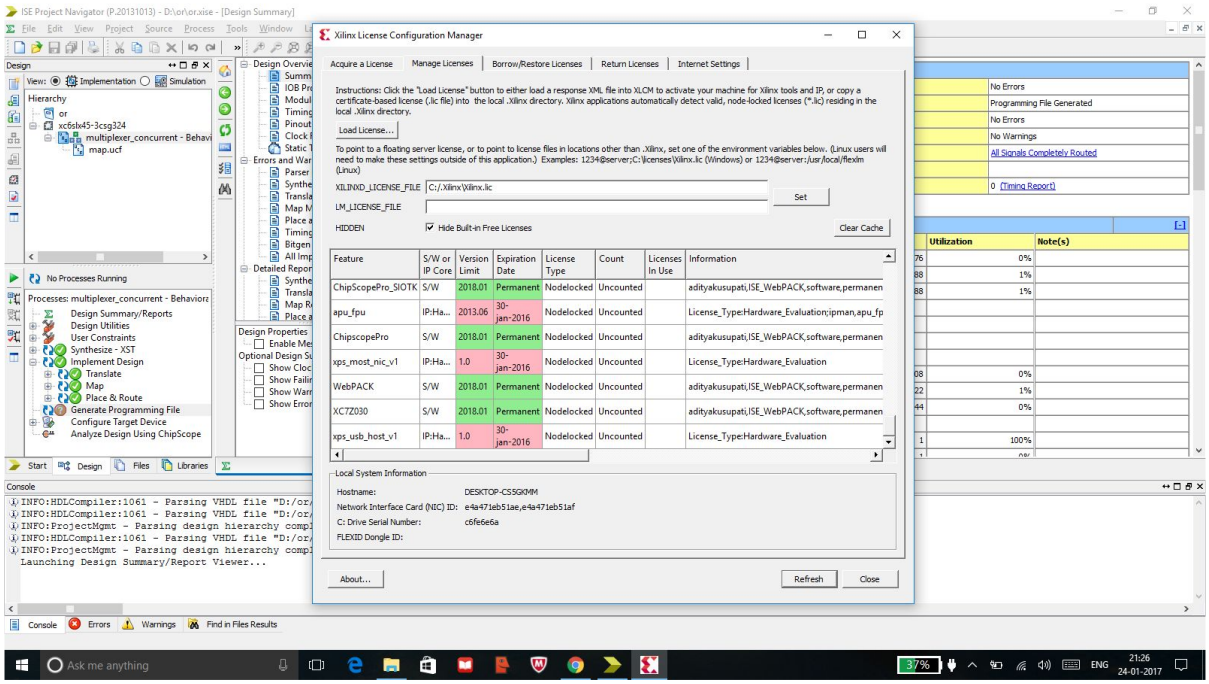
Linux Users : Use **sudo**

Ensure that you select the right pack



Proceed with the installation as mentioned here:
http://www.xilinx.com/support/documentation/sw_manuals/xilinx14_7/irn.pdf

Incase you guys have already installed the ISE and have licensed it.
Ensure the license is for the Web Pack and will be as follows in manage license window if already loaded.



If you have it then you can skip the next section.

Licensing

- Signup onto XILINX (preferably with gpo email)
- Goto https://secure.xilinx.com/webreg/register.do?group=esd_oms&tab=CreateLicense to get the license
- Select the ISE Webpack License only.
- If you don't see it, Check the Manage licenses tab for the ISE Webpack License
- The license will be emailed to your registered email ID.
- Download the license (Xilinx.lic)
- For Linux,
    - Copy the Xilinx.lic file to *<Xilinx_Installation_Directory>/14.7/ISE_DS/ISE/coregen/core_licenses*
- For Windows,
    - Open License manage
    - Browse and select your License file (Xilinx.lic)

Installing Adept2

Windows

- Download Adept from http://www.cse.iitb.ac.in/~supratik/courses/cs254/digilent.adept.system_v2.16.4.exe
- Install both the exe by double clicking and following further instructions.

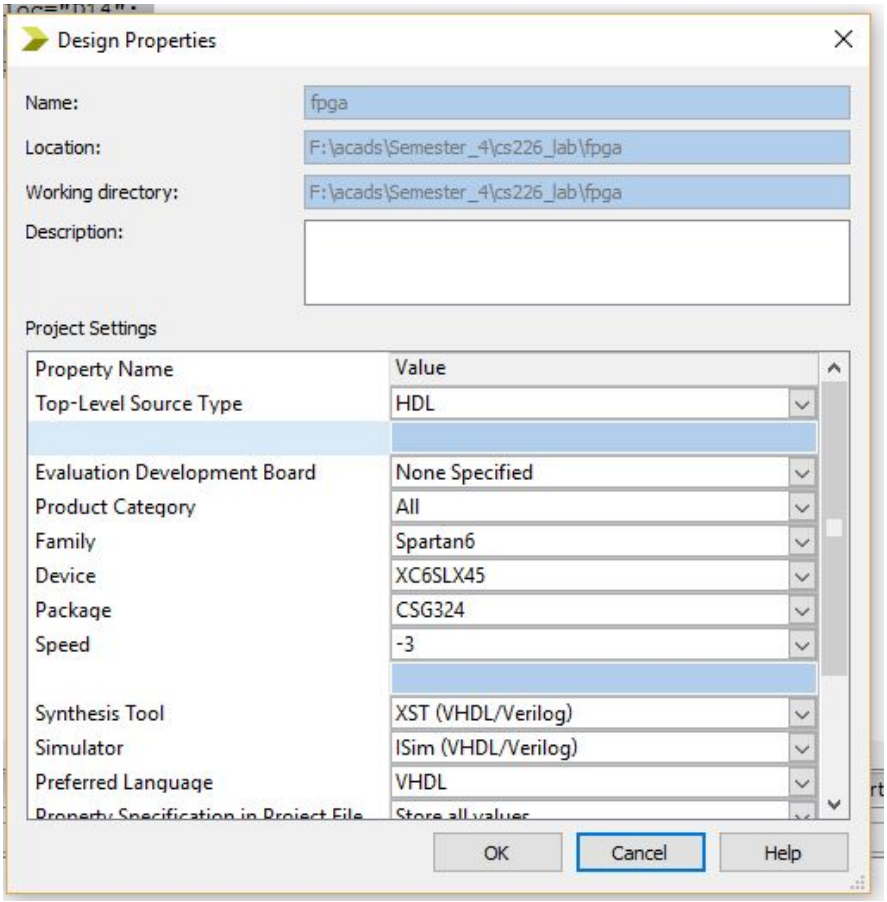
Ubuntu

- Download the Ubuntu Runtime, Linux Utilities tar-zips from the course Webpage.
- For each of them,
    - Extract
    - Run $ sudo ./install.sh
- Follow the installation guidelines from the link provided on the course webpage, replacing `Nexys3' with `Atlys' in all commands.

Burning onto FPGA

Step1: Ensure Design Properties

- RightClick Project -> Design Properties
- Ensure your design properties are exactly the same. Refer to the screenshot below:



Step2 : Write the Implementation constraints file

- Make a new Source file by right clicking on the top module.
- Type of your file should be “Implementation constraints file”
- Map the ports appropriately as given in example below:-

Net "a" loc="A10";
Net "b" loc="D14";
Net "res" loc="U18";
Net "carry" loc="M14";

Where a,b are input signals and res carry are output signals
A10, D14 are black switch ids
U18,M14 are Led ids

Step4:

- Synthesize -> Implement Design -> Generate Programming file .

Step5:

- Connect fpga board to your machine

Step6: Burning the Board (not literally)

(Windows)

- Start Adept and you would find a option to connect to atllys
- Click on Initialize chain
- Browse and add the .bit file and click Program.

(Linux)

- Install Adept2, if not already done so
- Finally, execute:

```
$ djtgcfg init -d  Atlys
$ djtgcfg prog -d Atlys -i 0 -f <filename>.bit
```

Step7:-

- Toggle FPGA switches to test.