

**Dr. Uday Khedker**

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## BIODATA

- **Qualifications**

- Ph.D. in Computer Science & Engineering, IIT Bombay (1995).  
Title of the thesis : *A Generalised Theory of Bit Vector Data Flow Analysis*.
- M.Tech. in Computer Science from Department of Computer Science, University of Pune with *A grade* (1989).
- B.E. in Electronics & Telecommunication Engineering from Government Engineering College, Jabalpur securing *1<sup>st</sup> Div. with distinction* (1986).
- H.S.S.C. from M. P. Board of Secondary Education with *6<sup>th</sup> rank in merit* (1981).

- **Areas of Interests**

- Programming Languages, Language Processors (special interest in Compilers).
- Computer Science Education.

- **Experience**

- *Research* : Over 18 years of research experience.
- *Teaching* : Over 15 years of teaching experience.  
(Over 5 years as a Reader at Dept. of Computer Science, University of Pune, as an Asst. Professor at Dept. of Computer Science and Engg., at IIT Bombay from May 2001 to March 2003, as an Associate Professor from April 2004 to March 2009, and as a Professor since then).

- **Honours and Distinctions**

- IBM Faculty Award 2007.

## TEACHING AND RESEARCH

- **Courses Taught**

Design and Implementation of Gnu Compiler Generation Framework, Program Analysis, Compiler Construction, Advanced Compilers, Systems Programming, Software Laboratory, Programming Paradigms, Introduction to Programming etc.

- **Research Areas**

Have been working in the area of optimising compilers for over 17 years. Current sub-areas of interest include Interprocedural Data Flow Analysis, Heap Reference Analysis, Pointer Analysis, Static Inferencing of Flow Sensitive Polymorphic Types, and Compiler Verification.

A recent research thrust involves improving the GNU Compiler Collection (GCC). With our studies, we have been able to bring down the ramp up period in GCC internals from six months to less than a month. Two important research goals in GCC are (a) To support automatic construction of machine dependent optimizers, and (b) to improve the instruction selection algorithms thereby simplifying the machine descriptions.

We have set up *GCC Resource Center* (<http://www.cse.iitb.ac.in/grc>) to explain our findings to GCC community. Two of our focussed activities involve (a) incorporating our precise, general, and efficient interprocedural data flow analysis algorithms in GCC, and (b) simplifying machine descriptions by changing the instruction selection mechanism in GCC.

More details about my current research can be found in my presentation available at:

<http://www.cse.iitb.ac.in/uday/soft-copies/overview.pdf>

- **Publications**

- **Books**

Uday P. Khedker, Amitabha Sanyal, and Bageshri Karkare. *Data Flow Analysis: Theory and Practice*. CRC Press, USA, 2009.

- **Book Chapters**

1. Amitabha Sanyal and Uday P. Khedker. *Garbage Collection Techniques*. In “The Compiler Design Handbook : Optimizations & Machine Code Generation.” (2nd Ed.) CRC Press USA. 2007.
2. Uday P. Khedker. *Data Flow Analysis*. In “The Compiler Design Handbook : Optimizations & Machine Code Generation.” (1st Ed.) CRC Press USA. 2002.

- **Journal Papers**

1. Aditya Kanade, Amitabha Sanyal, and Uday P. Khedker. *Validation of GCC optimizers through trace generation*. Software Practice and Experience 39(6): 611-639 (2009).
2. Uday P. Khedker, Amitabha Sanyal, and Amey Karkare. *Heap reference analysis using access graphs*. ACM Transactions on Programming Languages & Systems. Vol. 30, Issue 1 (Nov. 2007).
3. Bageshri Sathe and Uday P. Khedker. *An improved bound for call-Strings based interprocedural data flow analysis*. ACM Transactions on Programming Languages & Systems. Vol. 29, Issue 6 (Oct. 2007).
4. Uday P. Khedker, D. M. Dhamdhere, and Alan Mycroft. *Bidirectional data flow analysis for type inferencing*. Computer Languages, 29(1-2), Pages 15-44, 2003.
5. Rahul Joshi, Uday P. Khedker, Vinay Kakade, and Medha Trivedi. *Some interesting results about applications of graphs in compilers*. CSI Journal, 31(4), 2002.
6. Uday P. Khedker and D. M. Dhamdhere. *Bidirectional data flow analysis : Myths and reality*. SIGPLAN Notices, June 1999.

7. Uday P. Khedker and D. M. Dhamdhere. *A generalized theory of bit vector data flow analysis*. ACM Transactions on Programming Languages & Systems, 16(5):1472–1511, 1994.
- **Conference and Workshop Papers**
1. Rupesh Nasre, Kaushik Ranjan, R. Govindrajan, and Uday P. Khedker. *Scalable context-sensitive points-to analysis using multi-dimensional bloom filters*. Asian Symposium on Programming Languages and Symposium (APLAS 2009). Korea, (Dec 2009).
  2. Uday Khedker and Bageshri Sathe. *Efficiency, precision, simplicity, and generality in interprocedural data flow analysis: resurrecting the classical call strings method*. International Conference on Compiler Construction (CC 2008), Budapest, Hungary.
  3. Sameera Deshpande and Uday P. Khedker. *Incremental machine descriptions for GCC*. International Workshop on GCC for Research in Embedded Parallel Systems (GREPS'07) held in conjunction with International Conference on Parallel Architectures and Compilation Techniques (PACT 2007). September 2007, Brasov, Romania.
  4. Amey Karkare, Uday P. Khedker and Amitabha Sanyal. *Liveness of heap data for functional programs*, Heap Analysis and Verification Workshop. In the European joint conferences on Theory And Practice of Software (ETAPS'07), Vienna, Austria.
  5. Aditya Kanade, Amitabha Sanyal, and Uday P. Khedker. *A PVS based framework for validating compiler optimizations*. The 4th IEEE International Conference on Software Engineering and Formal Methods (SEFM'06), Pune, India, September 11-15, 2006.
  6. Bageshri Sathe and Uday P. Khedker. *Complexity of data flow analysis for non-separable frameworks*. The 2006 International Conference on Programming Languages and Compilers (PLC'06), June 26-29, 2006, Las Vegas, USA.
  7. Bageshri Sathe and Uday P. Khedker. *Static Program partitioning for embedded processors*. The 2006 International Conference on Embedded Systems and Applications. (ESA'06), June 26-29, 2006, Las Vegas, USA.
  8. Aditya Kanade, Amitabha Sanyal, and Uday P. Khedker. *Structuring optimizing transformations and proving them sound*. The 5th International Workshop on Compiler Optimization meets Compiler Verification (COCV'06), Pages 105-121. In the European joint conferences on Theory And Practice of Software (ETAPS'06), Vienna, Austria.
  9. Aditya Kanade, Uday P. Khedker and Amitabha Sanyal. *Heterogeneous fixed points with applications to points-to analysis*. 3rd Asian Symposium on Programming Languages and Systems (ASPLAS'05), Tsukuba, Japan, 2005. Volume 3780 of Lecture Notes in Computer Science, Springer-Verlag.
  10. Uday P. Khedker and R. Govindarajan. *Compiler analysis and optimizations : What is new?* Invited paper. Proceedings of the Workshop on Cutting Edge Computing (New Frontiers in High Performance Computing). Pages 59-69. International Conference on High Performance Computing (HiPC03), Hyderabad, 2003.
  11. D. M. Dhamdhere and Uday P. Khedker. *Complexity of bidirectional data flow analysis*. In Proceedings of the 20<sup>th</sup> Annual ACM SIGACT/SIGPLAN Symposium on Principles of Programming Languages, Charleston, South Carolina, (USA), January 11–14, 1993.
- **Miscellaneous Papers**
1. Amey Karkare, Amitabha Sanyal, and Uday P. Khedker. *Effectiveness of garbage collection in MIT/GNU Scheme*. ACM Computing Research Repository (abs/cs/0703155) November, 2006.

## PROJECTS AND CONSULTANCY ASSIGNMENTS

Have been a consultant to many companies. The work usually involves training and grooming compiler groups, advising on design issues for compiler related projects etc.

- **Trainings**

- *Workshop on Compiler Construction with Introduction to GCC*. IIT Bombay, Mumbai. (Dec 2009).
- *Compiler Back Ends*. (With Prof. Amitabha Sanyal). TCS, Hyderabad. (Sept. 2009).
- *Compiler Construction: From Practice to Theory*. A workshop under Faculty Development Program of TCS at Pune. (Feb 2009).
- *Compiler Construction: From Practice to Theory*. IITDM, Jabalpur. (Dec 2008).
- *Compiler Construction: From Practice to Theory*. A TEQIP (Technical Quality Improvement Program) workshop at College of Engineering, Pune. (Sept 2007).
- *Automatic Construction of Scanners and Parsers*. Blue Star Infotech Ltd. (Mumbai). (Feb 2007)
- *Getting Started with Porting GCC*. (With Prof. Amitabha Sanyal and Prof. Supratim Biswas). Infineon (Bangalore). (Feb 2004)
- *Compiler Construction*. (with Prof. Amitabha Sanyal and Prof. Supratim Biswas). ANURAG, a DRDO lab (Hyderabad). (December 2003)
- *Compiler Back Ends*. (With Prof. Amitabha Sanyal). Synopsys India (Pvt.) Ltd. (December 2002).
- *Ada Programming Language*. (With Prof. H. V. Sahasrabudhe). Jopasana Software & Systems Pvt. Ltd. (May 2001)
- *Data Flow Analysis*. Tata Infotech Ltd. (December 1999).
- *Language Processing*. Tata Infotech Ltd. (December 1998).
- *Low Level Language Processing Tools*. Cirrus Logic Software (I) Pvt. Ltd. (November 1998).
- *Language Design and Compiler Construction*. Mastek, Pune. (Dec 1996 to May 1997).
- *Bidirectional Data Flow Analysis*. TRDDC, Pune (May 1996 to July 1996).

- **Sponsored Projects**

- *Trusted Translation Systems*. (With Prof. Amitabha Sanyal and Prof. S. Biswas). Centre for Formal Design and Verification of Software. (December 2003 to Dec 2008).
- *Improving GCC port for ANUPAMA and ABACUS processors*. (With Prof. Amitabha Sanyal and Prof. S. Biswas). Sponsored by ANURAG, DRDO. (December 2004 to March 2006).
- *Heap reference analysis for improved garbage collection*. Sponsored by Synopsys India (Pvt.) Ltd. (May 2003 to June 2004).
- *Retargeting of GNU C/C++ compiler and associated tools for ARC100 and ARC200 RISC cores*. Sponsored by ARCUS Technologies Pvt. Ltd., Bangalore (May 1994 to November 1994).

- **Consultancy Projects**

- *PL/I to C++ Translation.* (With Prof. Amitabha Sanyal). Patni Computer Systems, Pune (March 2009 to April 2009).
- *Efficient programming with GCC for Tricore.* (With Prof. Amitabha Sanyal and Prof. S. Biswas). Sponsored by Infineon Technologies Ltd., Bangalore (July 2005 to January 2006).
- Tuning of *lcc* for better code generation for UMS chip of Cradle Technologies Ltd. (December 2000 to May 2001).
- Was the chief designer of VxC designed by Tata Infotech Ltd. This is a variant of C for embedded systems applications of Intel (September 2000 Jan 2002).

- Was the principal architect of an optimizing compiler for VxC designed and implemented by Tata Infotech Ltd. for Intel's IXS 1000 Media Signal Processor (September 2000 Jan 2002).

Some features of this instruction set architecture are : Asymmetric vector and scalar units, generalisation of MAC operation concept, predicated instructions, restricted VLIW architecture with short as well as long instructions, manipulation of data during memory reads and writes, parallel loads and stores, local customisation of execution semantics etc.

- Have carried out the feasibility study for design and implementation of an optimizing compiler for Intel's DSP chip on behalf of Tata Infotech Ltd. (June 2000)
- Have carried out a feasibility study on rapid software development for DSP chips for Cirrus Logic Software (I) Pvt. Ltd. (May 1998 to June 1998).

## RESEARCH TALKS AT PRESTIGIOUS INSTITUTIONS AND FORA

Have given numerous motivational, popular, technical talks at over 50 colleges and institutions in India. These talks try to explain what research is in general, what are its implications and requirements etc.

Have also delivered research and invited talks at many companies, institutions and conferences. These institutions include University of Cambridge, University of California at Berkeley, various IITs and IISc, Rutgers University, CWI (Amsterdam), Dagstuhl Seminar, INRIA etc. Companies where I have delivered research talks include IBM, HP, Synopsys, Motorola, Tata Infotech, Persistent Systems, Symantec etc.

## OTHER PROFESSIONAL ACTIVITIES

- Co-organiser of workshop on *New Horizons in Compilers* in conjunction with International Conference on High Performance Computing (HiPC), for past four years.
- Program committee International Conference on High Performance Computing (HiPC), 2006.
- Reviewer for ACM TOPLAS, POPL, PLDI, SAS, etc.
- Have been a member of Board of Studies in Computer Science at University of Mumbai, College of Engineering Pune, College of Engineering Aurangabad, Amravati University, Rani Durgawati Vishwavidyalaya, Jabalpur etc.
- Member of selection committees for faculty selection in various colleges.