# Ashutosh Gupta (January 2025)

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#### Research Interests

Formal methods and AI: Safety-critical learned systems

Verification: formal verification of sequential and concurrent software, invariant generation

Synthesis: automated generation of program code

Constraint solving: constraint logic programming, decision procedures, automated theorem proving

Modelling: modelling of biological systems, e.g., gene regulation

## **Academic Positions**

02/2018—now Associate Professor Indian Institute of Technology Bombay
11/2014—02/2018 Reader Tata Institute of Fundamental Research
4/2011—11/2014 PostDoc Institute of Science and Technology Austria

#### Education

3/2007–3/2011 PhD Computer Science Technische Universität München (TUM)

9/2005–3/2007 MS Computer Science École Polytechnique Fédérale de Lausanne (EPFL) 7/2000–5/2004 B.Tech. Electrical Eng. Indian Institute of Technology, Kanpur (IITK)

# **Industry Experience**

11/2008-1/2009 Intern Microsoft research

7/2005–9/2005 Design Engineer Whirlybird Electronics, Kanpur 6/2004–6/2005 Software Engineer ST Microelectronics, Noida

## PhD Thesis

Constraint solving for verification

# Awards

- $1.\,$  Gold medal in SV-COMP 2020, the competition on software verification
- 2. Best paper award at the 18th European Joint Conference on Theory and Practice of Software, 2015
- 3. Bronze/Gold medals in the concurrency track of the competition on software verification in 2012/2013
- 4. PhD Thesis prize 2011, Alumni association TUM (weblink)
- 5. Best paper award at the 12th European Joint Conference on Theory and Practice of Software, 2009

#### Grants

- 1. Towards trustworthy and verifiable AI for safety-critical systems, SBI foundation
- 2. Efficient automated synthesis of heart pacemaker from logical specifications, Trust Lab
- 3. Automated tools for programs with weak memory, MPG partners group with MPI-SWS
- 4. Efficient verification of concurrent programs, Start-up grant, SERB

#### Verification software

- 1. Diffy/Vajra: a tool for analyzing programs with arrays. (weblink)
- 2. LLVM BMC: a bounded model checker library for LLVM byte code. We developed the tool to be used as back-end of various tools. (weblink)
- 3. TARA: A concurrent traces analysis tool (weblink)
- 4. HSF: A Software Verifier based on Horn Clauses (weblink)
- 5. Threader: A model-checker for multi-threaded programs
- 6. CLP(Q+UIF)+Interpolation: constraint logic programming solver and interpolation procedure for combination of linear inequalities and uninterpreted function symbol
- 7. InvGen: An efficient invariant generator
- 8. TnT: An automated (non)-termination prover

#### **Edited Volumes**

1. CMSB : Proceedings Conference Computational Methods in Systems Biology 2013 Lecture Notes in Computer Science 8130 with Thomas A. Henzinger

## Refereed Conference Papers

Papers are available at https://www.cse.iitb.ac.in/~akg/. In the area of verification, names are written in alphabetical order, therefore the order of names has no meaning

- 1. Dynamic Partial Order Reduction for Transactional Programs on Serializable Platforms ATVA: Automated Technology for Verification and Analysis 2024. with Parosh Abdulla, Krishna S and Omkar Tuppe
- 2. Modelling Task Priority in Symbolic Predictive Analysis for Embedded Software Ada-Europe AEiC 2024 with Ranjani Krishnan
- 3. LTL-Based Non-Markovian Inverse Reinforcement Learning AAMAS: International Conference on Autonomous Agents and Multiagent Systems 2023 with Mohamed Afzal, Sankalp Gambhir, Krishna S, Ashutosh Trivedi, A. Velasquez
- 4. Optimal Stateless model checking for causal consistency TACAS: Tools and Algorithms for the Construction and Analysis of Systems 2023 with Parosh Abdulla, Mohamed Atig, Krishna S, and Omkar Tuppe.
- 5. Correct-by-Construction Reinforcement Learning of Cardiac Pacemakers from Duration Calculus Requirements

AAAI: Association for the Advancement of Artificial Intelligence Conference 2023 with Kalyani Dole, John Komp, Krishna S, and Ashutosh Trivedi.

- Event-Triggered and Time-Triggered Duration Calculus for Model-Free Reinforcement Learning, RTSS: Real-Time Systems Symposium 2021
   Kalyani Dole, John Komp, Krishna S, and Ashutosh Trivedi.
- Automated inference of production rules for glycans, CMSB: Computational Methods in Systems Biology 2021 Ansuman Biswas, Meghana Missula, Mukund Thattai.
- 8. Diffy: Inductive Reasoning of Array Programs using Difference Invariants. CAV : Computer Aided Verification 2021

with Supratik Chakraborty and Divyesh Unadkat

9. Robust Controller Synthesis for Duration Calculus, ATVA: Automated Technology for Verification and Analysis 2020. with Kalyani Dole and Krishna S.

10. VeriAbs: Verification by Abstraction and Test Generation (Competition Contribution). TACAS: Tools and Algorithms for the Construction and Analysis of Systems 2020 with M. Afzal, S. Chakraborty, A. Chauhan, B. Chimdyalwar, P. Darke, S. Kumar, C. Babu M, D. Unadkat, and R. Venkatesh.

11. Verifying Array Manipulating Programs with Full-Program Induction, TACAS: Tools and Algorithms for the Construction and Analysis of Systems 2020 with Supratik Chakraborty and Divyesh Unadkat

12. Synthesis for vesicle traffic systems,

CMSB: Computational Methods in Systems Biology 2018 with Somya Mani and Ankit Shukla.

13. SAT solving for vesicle traffic systems in cells, SASB: Static Analysis in System Biology 2017 with Ankit Shukla, Mandyam Srivas, and Mukund Thattai.

 Verifying Array Manipulating Programs by Tiling, SAS: Static Analysis Symposium 2017 with Supratik Chakraborty and Divyesh Unadkat

15. Matching multiplications in Bit-Vector formulas, VMCAI: Verification, Model Checking, and Abstract Interpretation 2017 with Supratik Chakraborty and Rahul Jain.

16. Abstraction-driven concolic testing,

VMCAI: Verification, Model Checking, and Abstract Interpretation 2016 with Przemyslaw Daca and Thomas Henzinger.

17. Model Checking Gene Regulatory Networks ( *Best paper award* ), TACAS: Tools and Algorithms for the Construction and Analysis of Systems 2015, with Mirco Giacobbe, Calin Guet, Thomas Henzinger, Tiago Paixao, and Tatjana Petrov

18. Succinct Representation of Concurrent Trace Sets

POPL: Principles of Programming Languages 2015 with Thomas Henzinger, Arjun Radhakrishna, Roopsha Samanta, and Thorsten Tarrach

19. Suraq - A Controller Synthesis Tool using Uninterpreted Functions,

HVC: Haifa Verification Conference 2014 with George Hofferek

20. Extensional Crisis and Proving Identity,

ATVA: Automated Technology for Verification and Analysis 2014 with Laura Kovacs, Bernhard Kragl and Andrei Voronkov

21. Tree Interpolation in Vampire,

LPAR-19: Logic for Programming Artificial Intelligence and Reasoning 2013 with Ragis Blanc, Laura Kovács, Bernhard Kragl

22. Synthesizing Multiple Boolean Functions using Interpolation on a Single Proof, FMCAD: Formal Methods in Computer Aided Design 2013 with Georg Hofferek, Bettina Könighofer, Jie-Hong Roland Jiang, and Roderick Bloem

23. Automatic linearizability proofs of concurrent objects with cooperating updates, CAV: Computer Aided Verification 2013 with Cezara Dragoi and Thomas Henzinger

24. Improved Single Pass Algorithms for Resolution Proof Reduction, ATVA: Automated Technology for Verification and Analysis 2012 also accepted as a poster at SAT 2012  Delayed Continuous Time Markov Chains for Genetic Regulatory Circuits, CAV: Computer Aided Verification 2012
 with Calin Guet, Thomas Henzinger, Maria Mateescu and Ali Sezgin

26. HSF(C): A Software Verifier based on Horn Clauses
TACAS (SV-COMP): the first model checking competition 2012
with Sergey Grebenshchikov, Nuno Lopes, Corneliu Popeea, and Andrey Rybalchenko

27. \*Solving Recursion-Free Horn Clauses over LI+UIF, APLAS: Asian Symposium on Programming Languages and Systems 2011 with Corneliu Popeea and Andrey Rybalchenko

28. Threader: A Constraint-based Verifier for Multi-Threaded Programs, CAV: Computer Aided Verification 2011 with Corneliu Popeea and Andrey Rybalchenko

 Predicate abstraction and refinement for verifying multi-threaded programs POPL: Principles of Programming Languages 2011 with Corneliu Popeea and Andrey Rybalchenko

30. Non-monotonic refinement of control abstraction for concurrent programs ATVA: Automated Technology for Verification and Analysis 2010 with Corneliu Popeea and Andrey Rybalchenko

31. Finding heap-bounds for hardware synthesis FMCAD: Formal Methods in Computer Aided Design 2009 with B. Cook, S. Magill, A. Rybalchenko, J. Simsa, S. Singh, and V. Vafeidais

32. InvGen: An efficient invariant generator CAV: Computer Aided Verification 2009 with Andrey Rybalchenko

33. From tests to proofs ( Best paper award )
TACAS: Tools and Algorithms for the Construction and Analysis of Systems 2009
with Rupak Majumdar and Andrey Rybalchenko

34. Proving non-termination

POPL: Principles of Programming Languages 2008 with Tom Henzinger, Rupak Majumdar, Andrey Rybalchenko, and Ru-Gang Xu

# Refereed Journal Papers

 Full-program induction: verifying array programs sans loop invariants STTT: Software Tools for Technology Transfer 2022 with Supratik Chakraborty, and Divyesh Unadkat

2. A formal methods approach to predicting new features of the eukaryotic vesicle traffic system Acta Informatica, 2019

with A. Bhattacharyya, L. Kuppusamy, S. Mani, A. Shukla, M. Srivas, and M. Thattai.

Model checking the evolution of gene regulatory networks
 Acta Informatica, 2016
 with Mirco Giacobbe, Calin Guet, Thomas Henzinger, Tiago Paixao, and Tatjana Petrov.

4. From tests to proofs

STTT: Software Tools for Technology Transfer 2013 with Rupak Majumdar and Andrey Rybalchenko

## Courses Offered

Data structures and algorithms 2023, 2024

 ${\bf Mathematical\ Logic\ 2020,} 2021,\ 2022,\ 2023$ 

Analysis of concurrent programs 2020,2021,2022,2023

Automated Reason 2018,2020,2021,2022,2024,2025

Automated reasoning and program verification 2015,2016,2019

Automata Theory 2019

Mathematical Logic 2015,2016

# Advisor for Master/Bachelor Theses

Namrita (PhD, ongoing)

Md. Afzal (PhD, ongoing)

Omkar Tuppe (PhD, ongoing)

Kalyani Dole (PhD)

Divyesh Unadkat ( PhD )

Rahul Jain (Masters Thesis, TIFR)

Shraddha Barke (B.Tech Thesis, BITS-Goa, India)

Shikhar Pandya (B.Tech Thesis, IET - Ahmadabad University, India)

Alexandre Thevenet (Masters thesis, ENS-Paris)