Ashutosh Gupta (March 2017)

Address: TIFR, Homi bhaba road, Colaba, Mumbai 400005, India
Email: agupta@tifr.res.in
Web: http://www.tcs.tifr.res.in/~agupta/ Phone/Fax: +91 22 2278 2997

Research Interests

Verification:	formal verification of sequential and concurrent software, invariant generation
Synthesis:	automated generation of program code
Constraint solving:	constraint logic programming, decision procedures, automated theorem proving
Modelling:	modelling of biological systems, e.g., gene regulation

Academic Positions

12/2014–now	Reader	Tata Institute of Fundamental Research
4/2011–11/2014	PostDoc	Institute of Science and Technology Austria

Education

3/2007–3/2011	PhD Computer Science	Technische Universität München (TUM)
9/2005–3/2007	MS Computer Science	École Polytechnique Fédérale de Lausanne (EPFL)
7/2000–5/2004	B.Tech. Electrical Eng.	Indian Institute of Technology, Kanpur (IITK)

Industrial Experience

7/2005–9/2005	Design Engineer	Whirlybird Electronics, Kanpur
6/2004–6/2005	Software Engineer	ST Microelectronics, Noida
5/2003–7/2003	Intern	Quazar Technologies, Delhi

PhD Thesis

Constraint solving for verification

Awards

1. Best paper award at the 18th European Joint Conference on Theory and Practice of Software, 4/2015
2. PhD Thesis prize 2011, Alumni association TUM (weblink)
3. Best paper award at the 12th European Joint Conference on Theory and Practice of Software, 4/2009

Grants

1. Automated tools for programs with weak memory, MPG partners group with MPI-SWS
2. Efficient verification of concurrent programs, Start-up grant, SERB

Software

1. TARA: A concurrent traces analysis tool (weblink)
2. HSF: A Software Verifier based on Horn Clauses (weblink)
3. Threader: A model-checker for multi-threaded programs
4. CLP(Q+UIF)+Interpolation: constraint logic programming solver and interpolation procedure for combination of linear inequalities and uninterpreted function symbol
5. InvGen: An efficient invariant generator
6. TnT: An automated (non)-termination prover

Edited Volumes

1. CMSB : Proceedings Conference Computational Methods in Systems Biology 2013
   Lecture Notes in Computer Science 8130
   with Thomas A. Henzinger

Refereed Conference Papers

Papers are available at http://ist.ac.at/~agupta. In the area of verification, names are written in alphabetical order, therefore the order of names has no meaning

1. Matching multiplications in Bit-Vector formulas,
   VMCAI: Verification, Model Checking, and Abstract Interpretation 2017
   with Supratik Chakraborty and Rahul Jain.
2. Abstraction-driven concolic testing,
   VMCAI: Verification, Model Checking, and Abstract Interpretation 2016
   with Przemyslaw Daca, Thomas Henzinger.
3. †Model Checking Gene Regulatory Networks (*Best paper award*),
   TACAS : Tools and Algorithms for the Construction and Analysis of Systems 2015,
   with Mirco Giacobbe, Calin Guet, Thomas Henzinger, Tiago Paixao, and Tatjana Petrov
4. *†Succinct Representation of Concurrent Trace Sets
   POPL : Principles of Programming Languages 2015
   with Thomas Henzinger, Arjun Radhakrishna, Roopsha Samanta, and Thorsten Tarrach
5. Suraq - A Controller Synthesis Tool using Uninterpreted Functions,
   HVC : Haifa Verification Conference 2014
   with George Hofferek
6. Extensional Crisis and Proving Identity,
   ATVA: Automated Technology for Verification and Analysis 2014
   with Laura Kovacs, Bernhard Kragl and Andrei Voronkov
7. Tree Interpolation in Vampire,
   LPAR-19: Logic for Programming Artificial Intelligence and Reasoning 2013
   with Ragis Blanc, Laura Kovcs, Bernhard Kragl
8. Synthesizing Multiple Boolean Functions using Interpolation on a Single Proof,
   FMCAD: Formal Methods in Computer Aided Design 2013
   with Georg Hofferek, Bettina Knighofer, Jie-Hong Roland Jiang, and Roderick Bloem
9. *†Automatic linearizability proofs of concurrent objects with cooperating updates,
   CAV: Computer Aided Verification 2013
   with Cezara Dragoi and Thomas Henzinger
10. *Improved Single Pass Algorithms for Resolution Proof Reduction,
    ATVA: Automated Technology for Verification and Analysis 2012
    also accepted as a poster at SAT 2012
11. *†Delayed Continuous Time Markov Chains for Genetic Regulatory Circuits,
    CAV: Computer Aided Verification 2012
    with Calin Guet, Thomas Henzinger, Maria Mateescu and Ali Sezgin
12. HSF(C): A Software Verifier based on Horn Clauses
    TACAS (SV-COMP): the first model checking competition 2012
    with Sergey Grebenshchikov, Nuno Lopes, Corneliu Popeea, and Andrey Rybalchenko

*Primary contributor
†Key Publications

13. *Solving Recursion-Free Horn Clauses over LI+UIF,
APLAS: Asian Symposium on Programming Languages and Systems 2011
with Corneliu Popeea and Andrey Rybalchenko
14. Threader: A Constraint-based Verifier for Multi-Threaded Programs,
CAV: Computer Aided Verification 2011
with Corneliu Popeea and Andrey Rybalchenko
15. *†Predicate abstraction and refinement for verifying multi-threaded programs
POPL: Principles of Programming Languages 2011
with Corneliu Popeea and Andrey Rybalchenko
16. Non-monotonic refinement of control abstraction for concurrent programs
ATVA: Automated Technology for Verification and Analysis 2010
with Corneliu Popeea and Andrey Rybalchenko
17. *Finding heap-bounds for hardware synthesis
FMCAD: Formal Methods in Computer Aided Design 2009
with B. Cook, S. Magill, A. Rybalchenko, J. Simsa, S. Singh, and V. Vafeidais
18. *InvGen: An efficient invariant generator
CAV: Computer Aided Verification 2009
with Andrey Rybalchenko
19. *†From tests to proofs (*Best paper award*)
TACAS: Tools and Algorithms for the Construction and Analysis of Systems 2009
with Rupak Majumdar and Andrey Rybalchenko
20. *†Proving non-termination
POPL: Principles of Programming Languages 2008
with Tom Henzinger, Rupak Majumdar, Andrey Rybalchenko, and Ru-Gang Xu

Refereed Journal Papers

1. From tests to proofs
STTT: Software Tools for Technology Transfer 2013
with Rupak Majumdar and Andrey Rybalchenko
2. Model checking the evolution of gene regulatory networks
Acta Informatica, 2016
with Mirco Giacobbe, Calin Guet, Thomas Henzinger, Tiago Paixao, and Tatjana Petrov.

Academic Projects

10/2008–12/2008	Automated computation of bound on resource consumption of C programs	Internship, MSRC Host: Byron Cook
8/2006–1/2007	Proving termination of program loops	Masters thesis, EPFL Advisor: Andrey Rybalchenko
2/2006–7/2006	Manufacturing of a DNA sensor chip	Semester Project, EPFL Advisor: Giovanni De Micheli

Advisor for Master/Bachelor Theses

Rahul Jain (Masters Thesis, TIFR)

Shraddha Barke (B.Tech Thesis, BITS-Goa, India)

Shikhar Pandya (B.Tech Thesis, IET - Ahmadabad University, India)

Alexandre Thevenet (Masters thesis, ENS-Paris)

Graduate level courses offered

Mathematical Logic 2015,2016

Automated reasoning and program verification 2015,2016

Teaching assistants

Introduction to functional programming and verification. Bachelor level course. 2010

Refereeing

2016: ICEC(PC member),

2015: FSTTCS(PC member), CMSB(PC Member), CAV, POPL

2014: LICS-CSL, CAV

2013: VMCAI, CMSB (PC member and Editor), LPAR

2012: CMSB, FMCAD, WING (PC Member)

2011: TACAS, ESOP, CAV, ESOP, WING-JSC

2010: APLAS, WING-JSC, CAV, POPL, SAS, LPAR

2009: CAV

References

Andrey Rybalchenko	Researcher, MSR Cambridge	rybal@microsoft.com
Thomas A. Henzinger	President, Institute of Science and Technology Austria	tah@ist.ac.at
Calin Guet	Professor, Institute of Science and Technology Austria	calin@ist.ac.at
Supratik Chakraborty	Professor, IIT Bombay, India	supratik@cse.iitb.ac.in