CASPER

CS305: Computer Architecture

Single Cycle CPU (Processor-101)

https://www.cse.iitb.ac.in/~biswa/courses/CS305/main.html

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Single Cycle Processor

- All operations – single cycle ☺
- Clock cycle (unit of time) will be defined based on the longest instruction.
- Two paths of interest: datapath and control. Control tells datapath what to do.
- Do not forget the stored program concept.

Clock Cycle

Tick, clock tick, clock period, clock, clock cycle, or cycle

Discrete time intervals

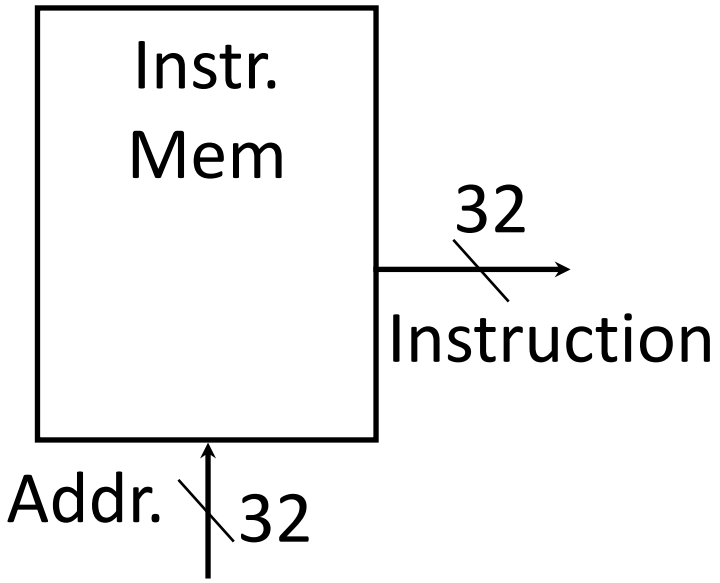
Based on processor frequency (clock rate)

1GHz processor, clock cycle = 1ns
4GHz processor, clock cycle = 0.25ns

Let’s start with the datapath

Anything that stores data or operates on data, within a processor

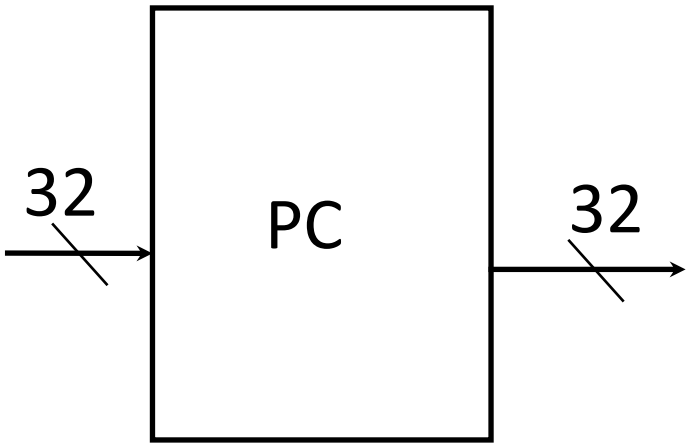
Instruction Memory



Remember: No writes to instruction memory ☺

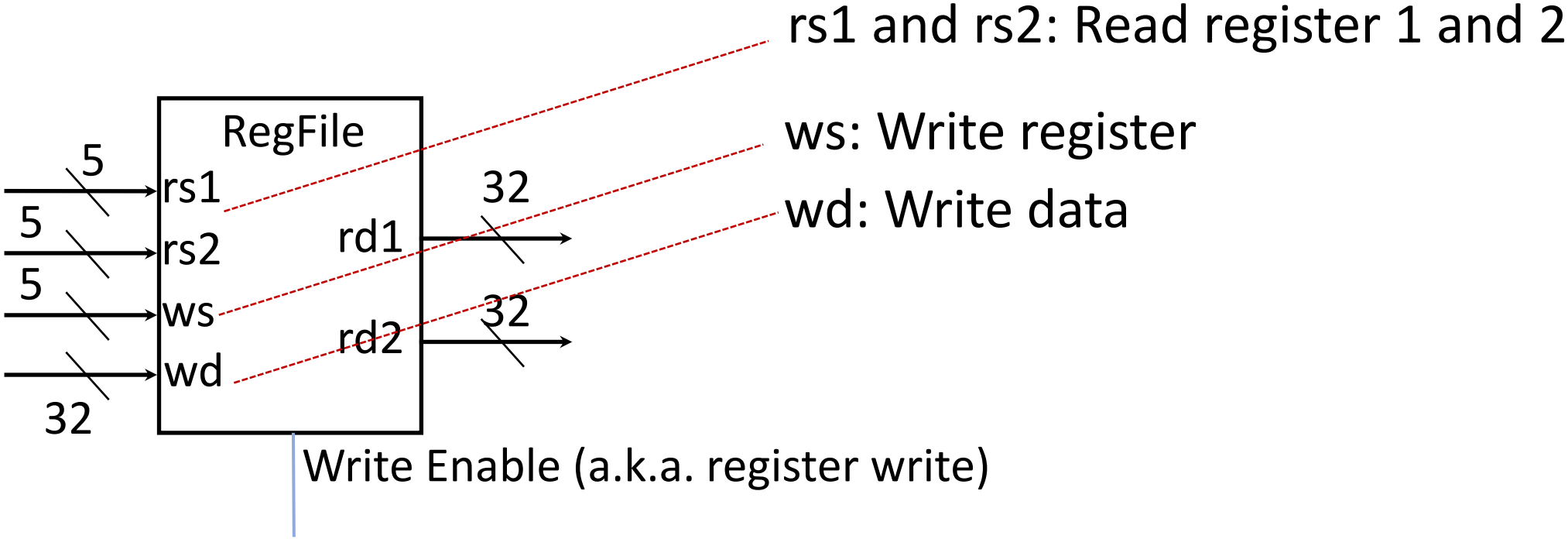
Not concerned about how programs are loaded into this memory.

Program Counter

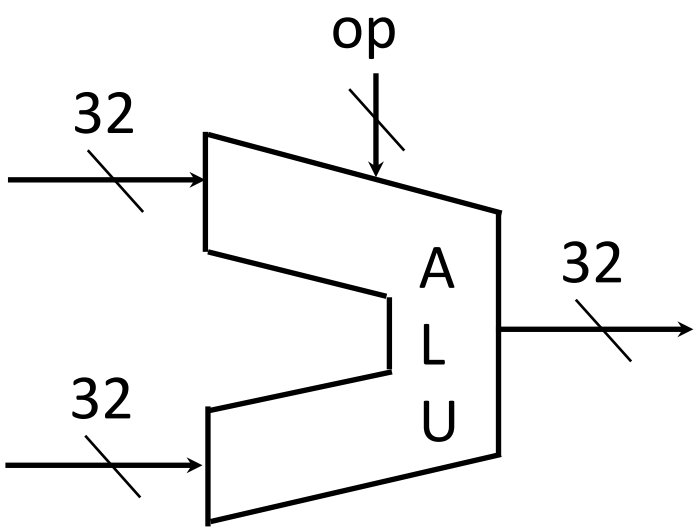


Remember: No writes to instruction memory ☺

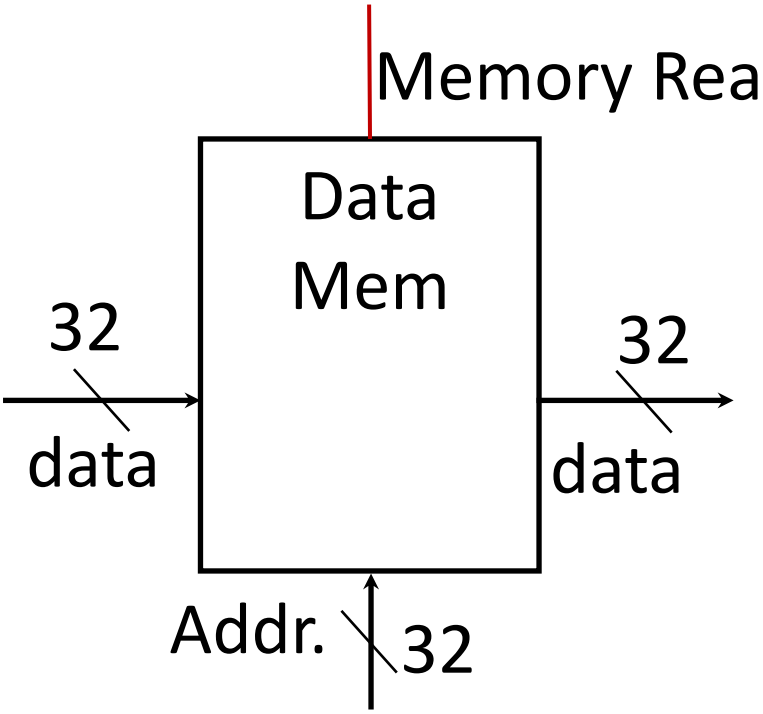
Register File



The ALU

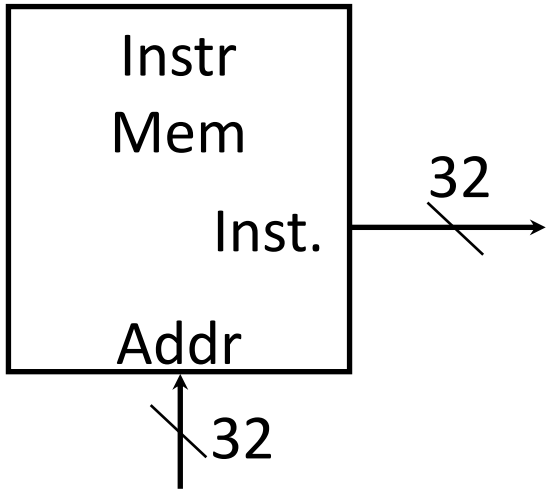


Data Memory

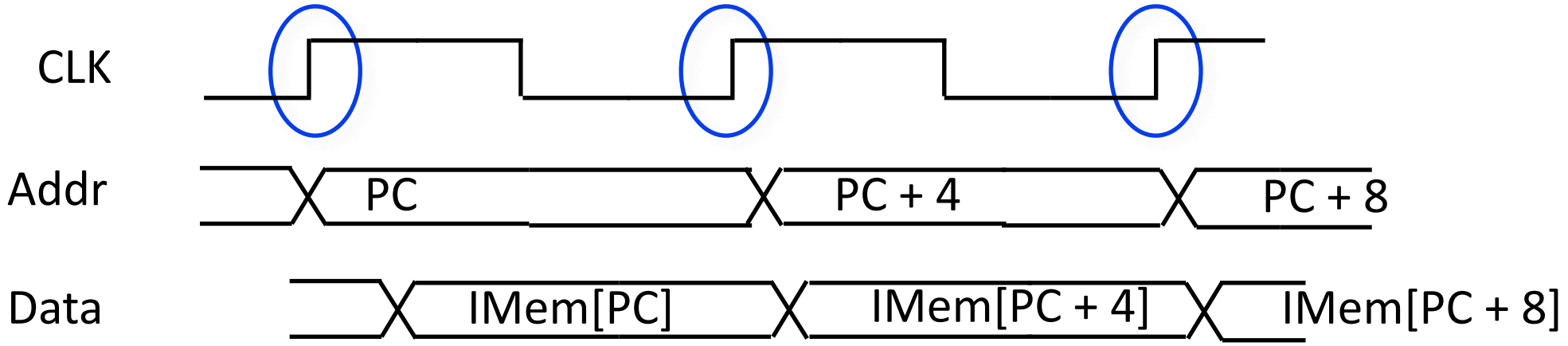


Why data and instruction memory and not one memory?
Discuss on Piazza

Address and Data Bus (Instruction Fetch)

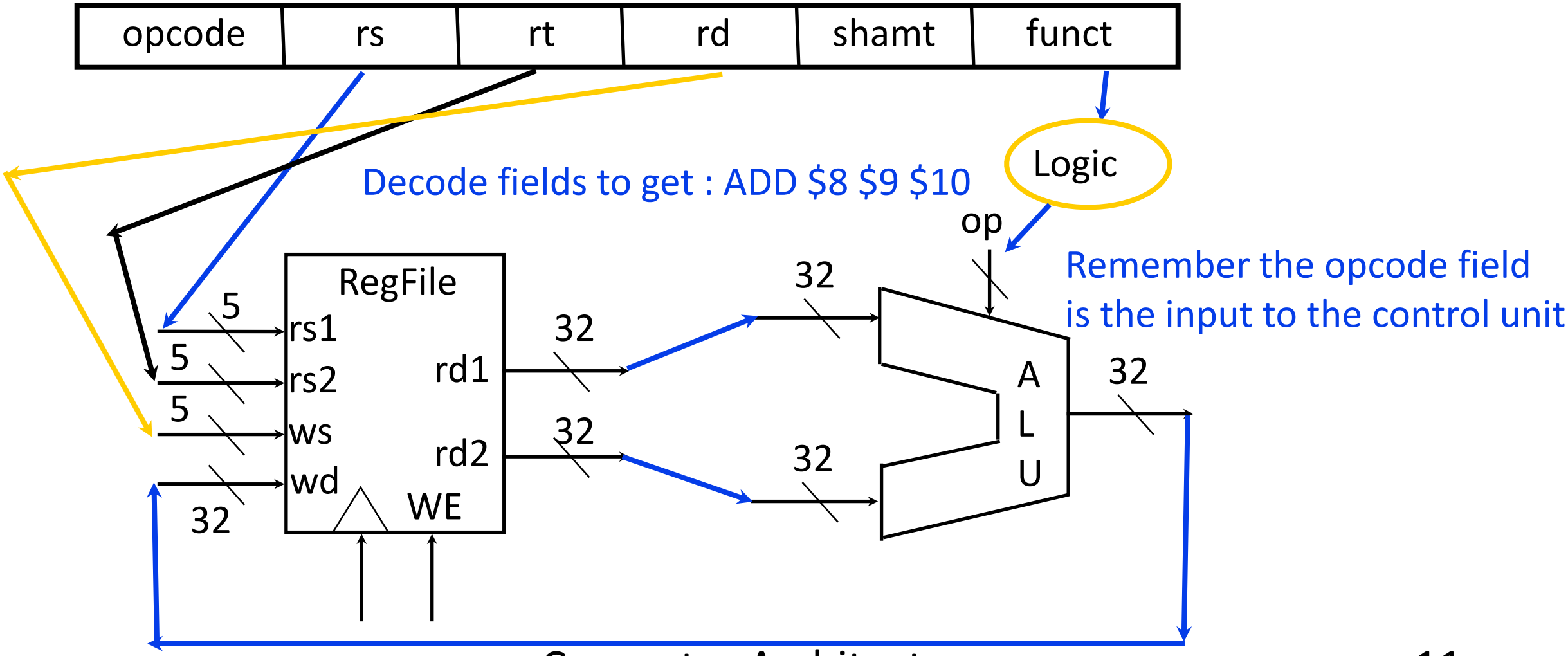


Fetching straight-line MIPS instructions requires a machine that generates this timing diagram:

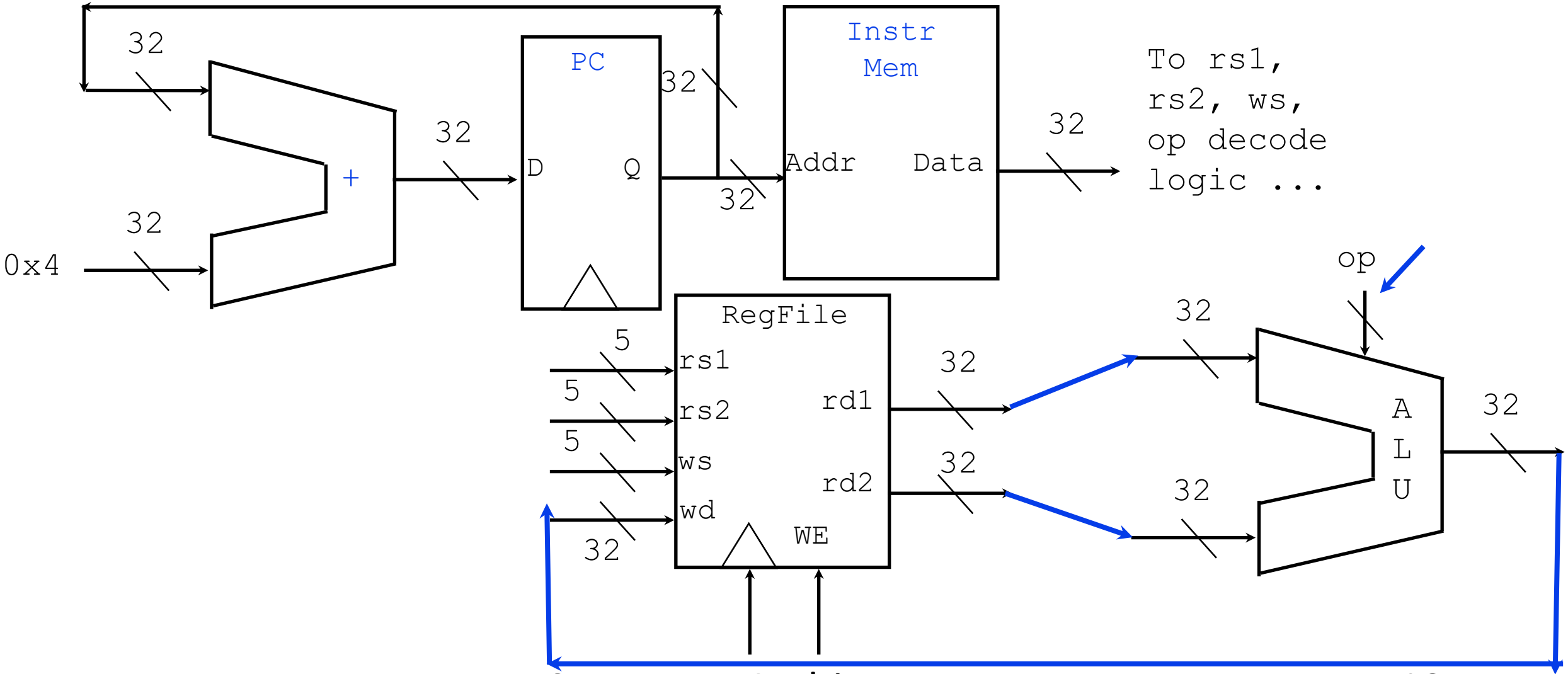


PC == Program Counter, points to next instruction.

Decode and Execute



All in one go


32
32
0x4
+
32
PC
D
Q
32
32
Instr
Mem
Addr
Data
32
To rs1,
rs2, ws,
op decode
logic ...
op
RegFile
5
5
5
32
rs1
rs2
ws
wd
rd1
rd2
WE
32
32
32
32
A
L
U
32

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