CS305: Computer Architecture

Single Cycle CPU cont.

https://www.cse.iitb.ac.in/~biswa/courses/CS305/main.html

https://www.cse.iitb.ac.in/~biswa/
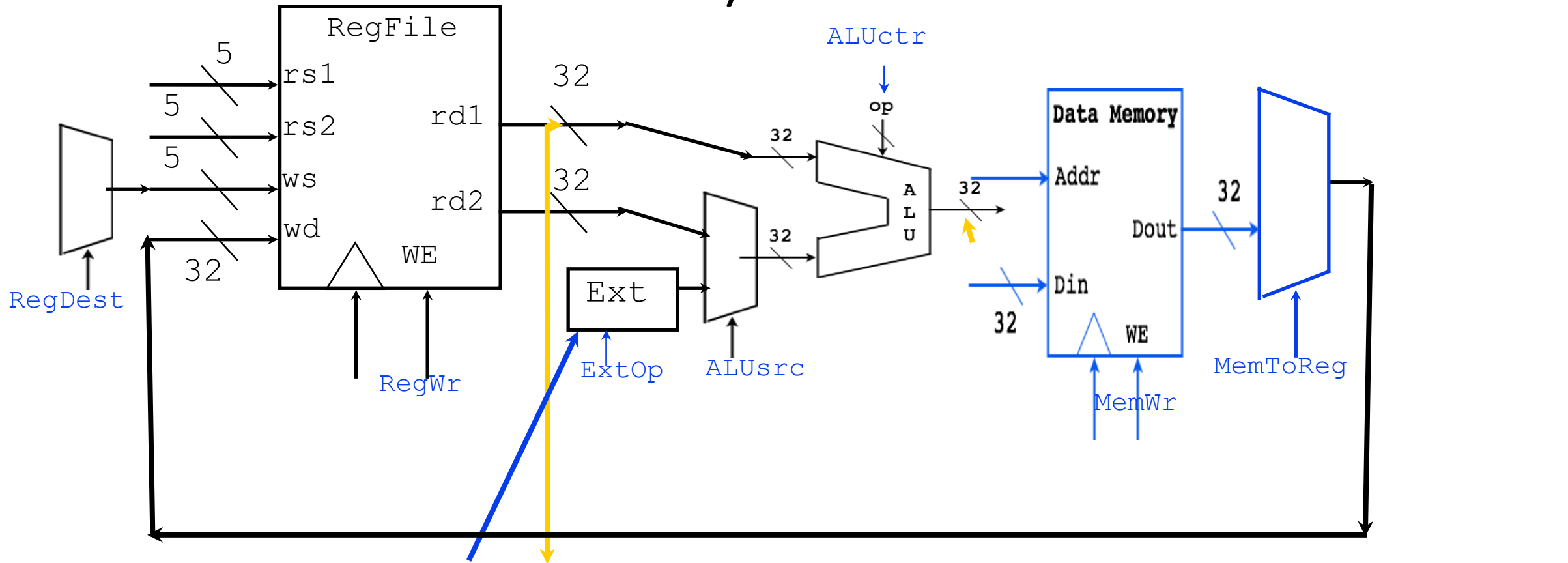
What about I format?
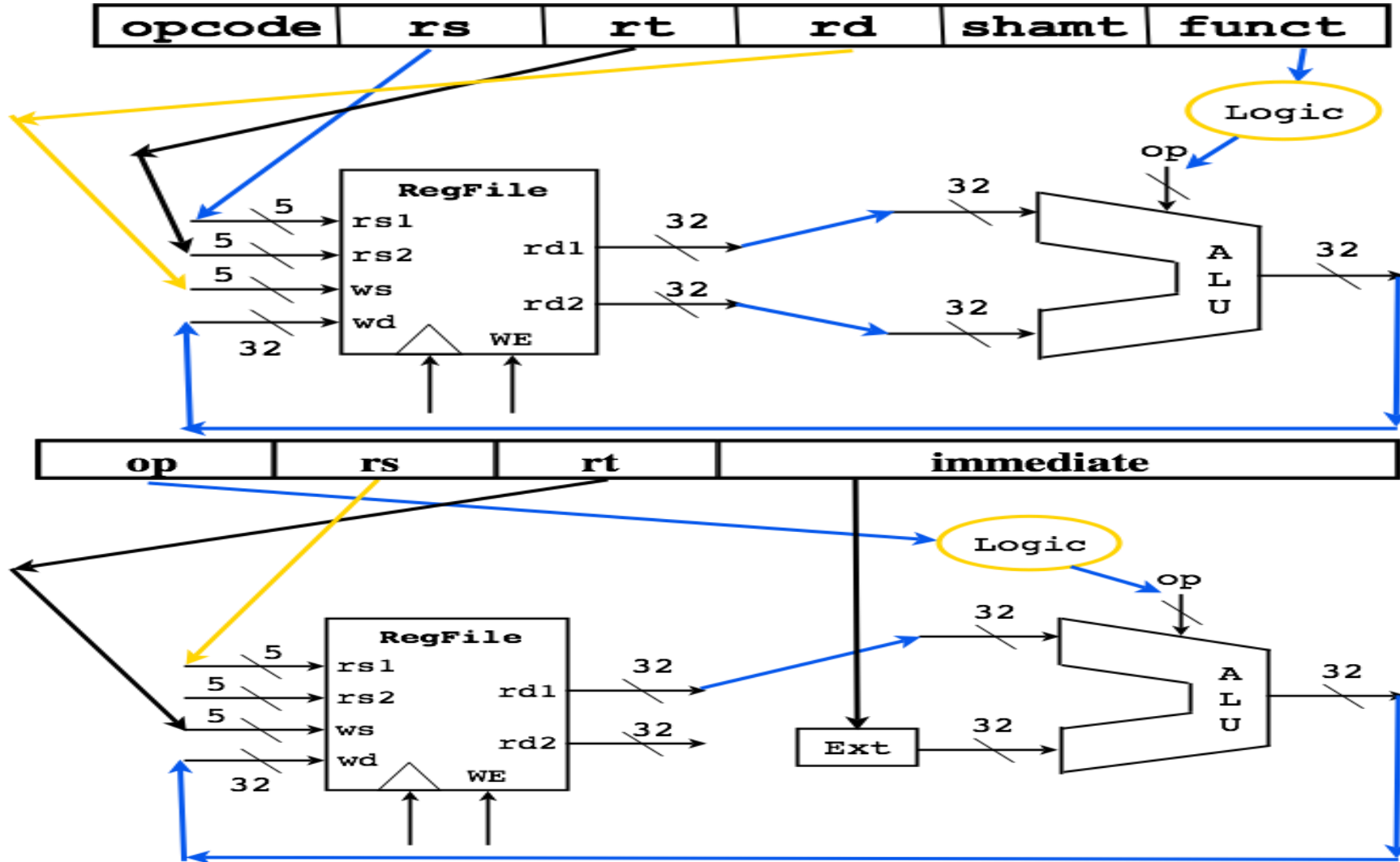
Loads from Memory

Syntax: LW $1, 32($2)   Action: $1 = M[$2 + 32]

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Control Signals So far

- MemRead

- MemWrite

- RegWrite

- MemtoReg

- RegDst

- ALUop, ALUSrc

- PCSrc (we have not discussed about the branch)

Read address | Instruction [31-0]

Instruction memory

I [31 - 26]

I [5 - 0]

Zero

Control
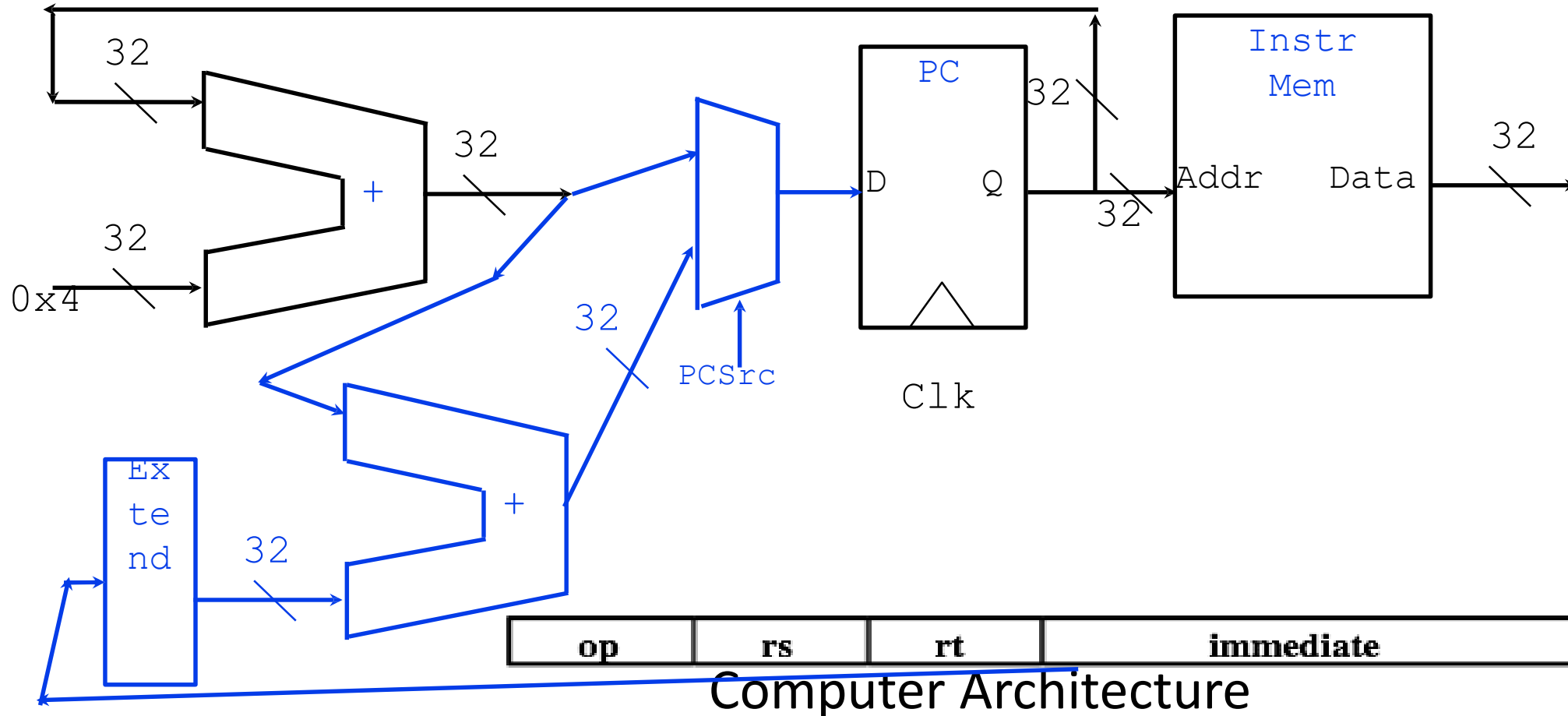
RegDst
RegWrite
ALUSrc
ALUOp
MemWrite
MemRead
MemToReg
PCSrc
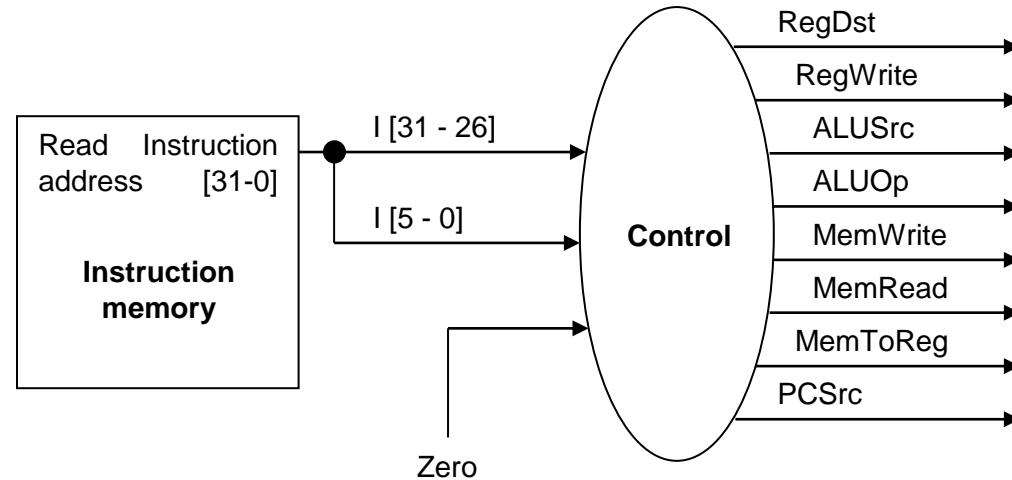
Branch Instructions

Syntax: BEQ $1, $2, 12
Action: If ($1 != $2), PC = PC + 4
Action: If ($1 == $2), PC = PC + 4 + 48

In detail

- MemRead: Read from memory when assert
- MemWrite: Write into the memory when assert
- RegWrite: Reg. on Write register updated with the input, on assert
- MemtoReg: On assert, memory to register, on deassert, ALU to register
- RegDst: On assert, use rd field, on deassert use rt field
- ALUSrc: On assert, lower 16 bits of an inst., on deassert from the second register
- PCSrc: On assert, branch target, deassert, PC+4

Control Signal Table

Operation	RegDst	RegWrite	ALUSrc	ALUOp	MemWrite	MemRead	MemToReg
add	1	1	0	010	0	0	0
sub	1	1	0	110	0	0	0
and	1	1	0	000	0	0	0
or	1	1	0	001	0	0	0
slt	1	1	0	111	0	0	0
lw	0	1	1	010	0	1	1
sw	X	0	1	010	1	0	X
beq	X	0	0	110	0	0	X

The Complete Picture

I[31-26]: Control unit

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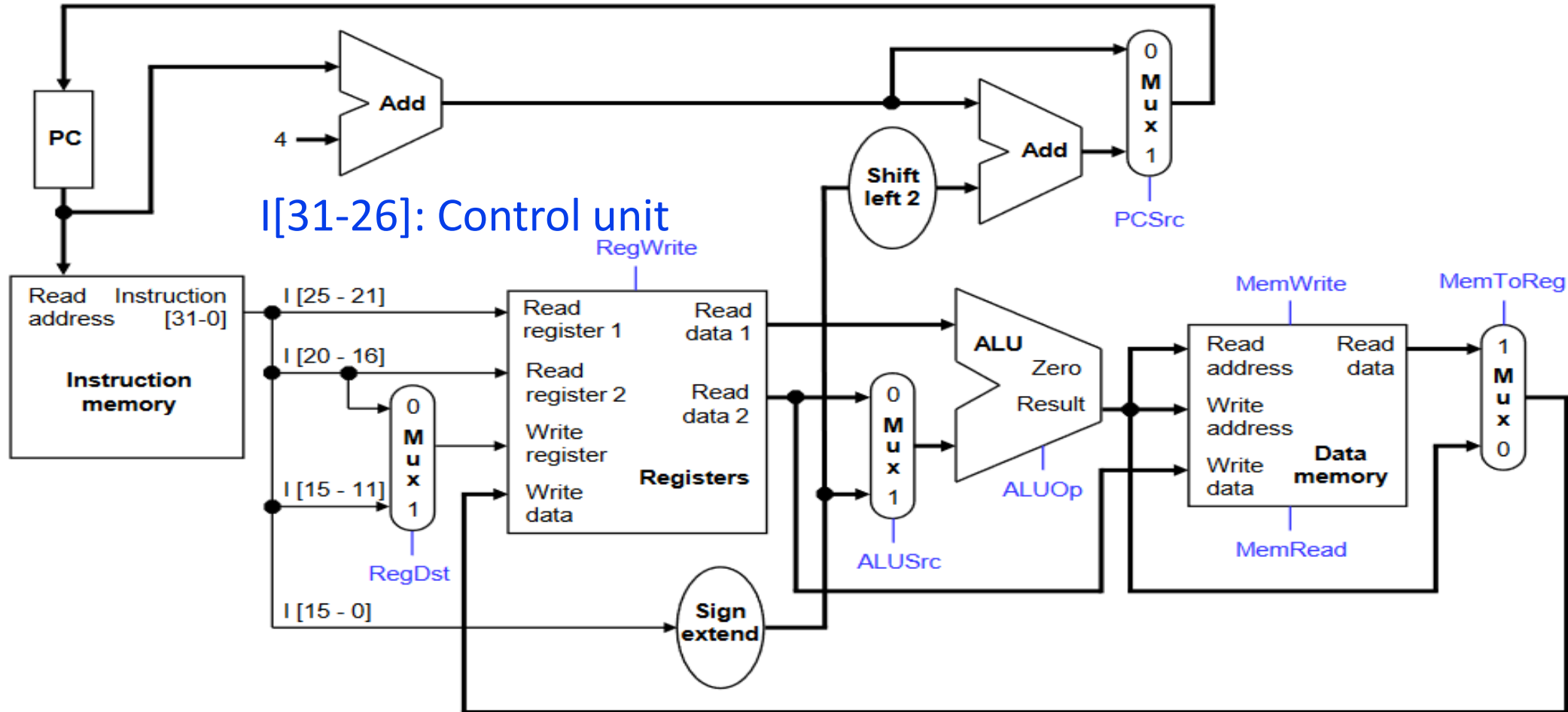
Why not single cycle?

• The longest possible datapath is the clock cycle time.
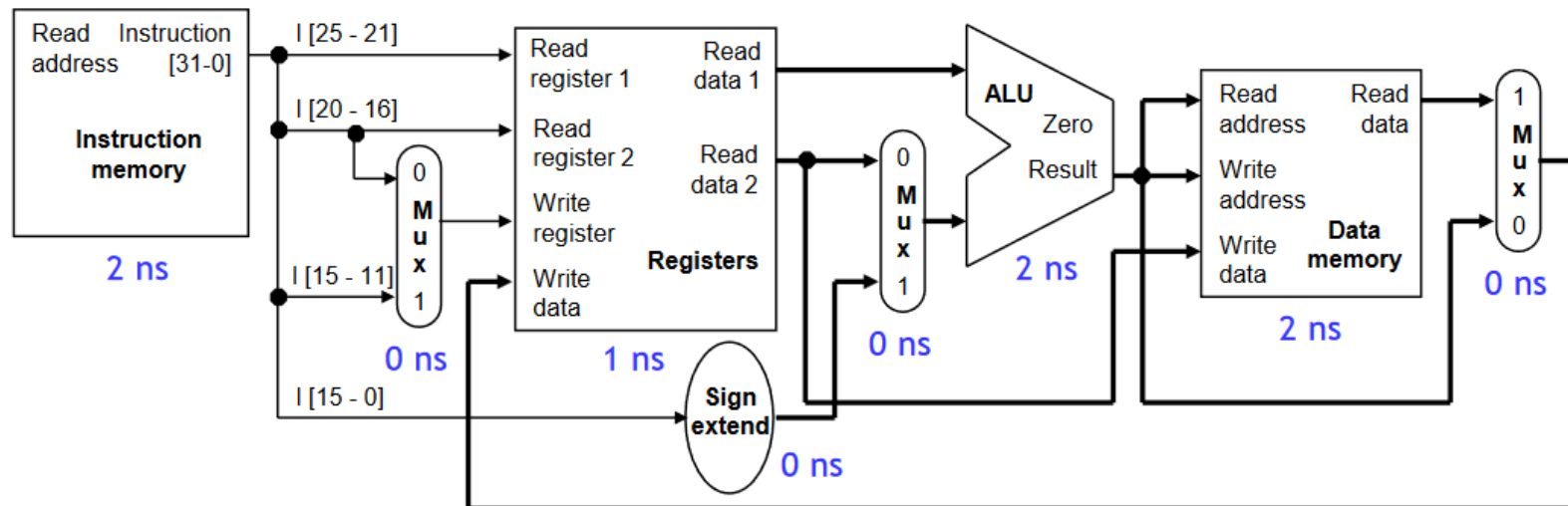
What does it mean?

Why not single cycle?

- For example, lw $t0, –4($sp) needs 8ns, assuming the delays shown here.

reading the instruction memory	2ns
reading the base register $sp	1ns
computing memory address $sp-4	2ns	8ns
reading the data memory	2ns
storing data back to $t0	1ns

one clock cycle: 8ns

Processor frequency: 125MHz

Cycle per Instruction (CPI): 1

An add instruction: no need of 8ns

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