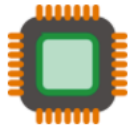


CASPER

CS305: Computer Architecture

Multi-Cycle CPU

https://www.cse.iitb.ac.in/~biswa/courses/CS305/main.html

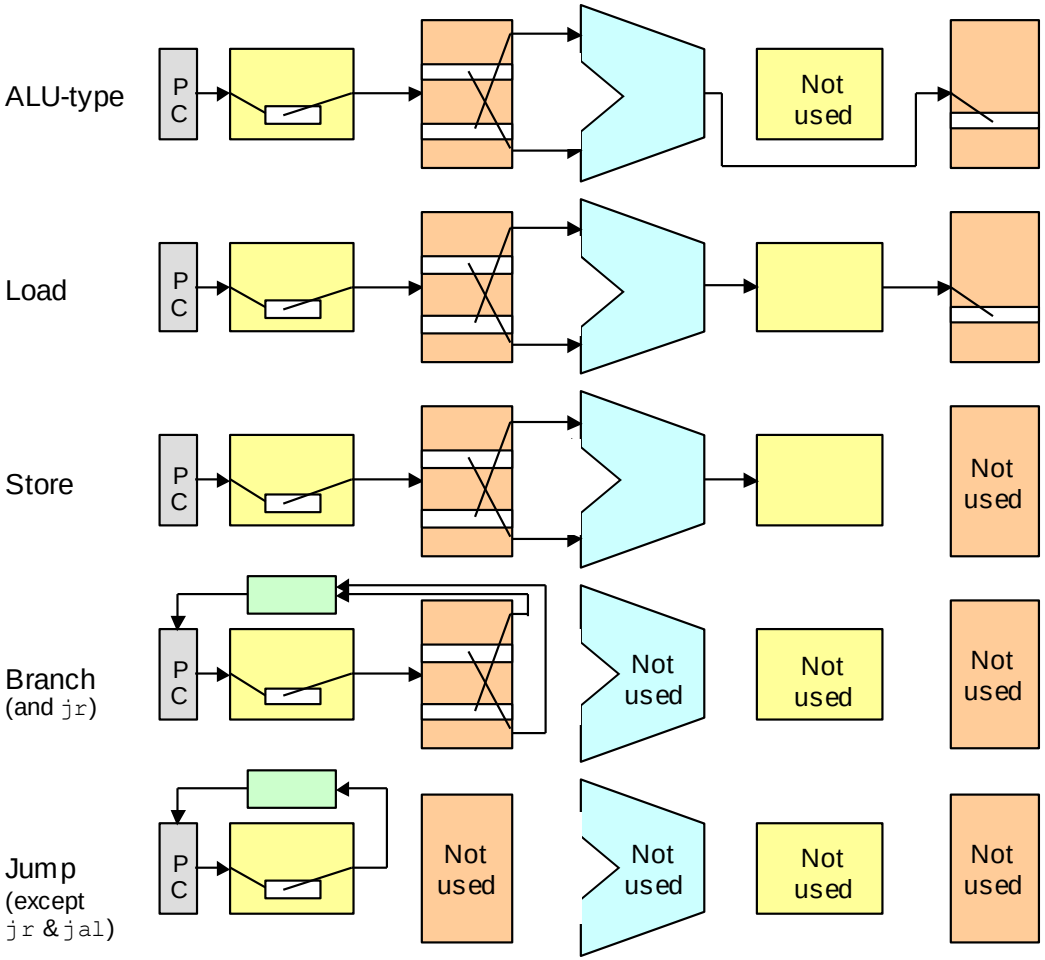
https://www.cse.iitb.ac.in/~biswa/

Why not single cycle?

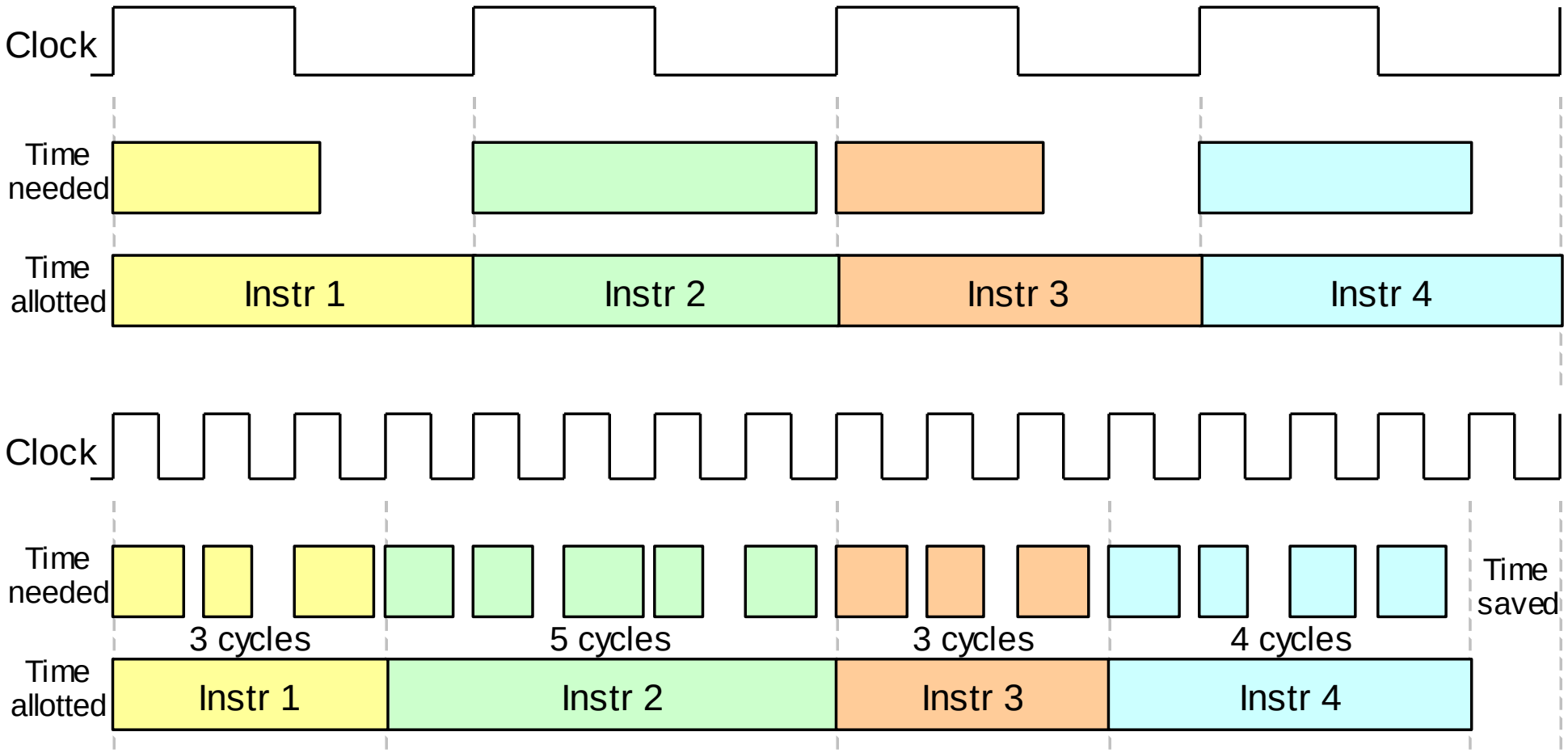
- The longest possible datapath is the clock cycle time.

Violating *common case fast (Confucius says)*

Oh No! Such a bad design



Single to Multi Cycle



Multicycle CPI

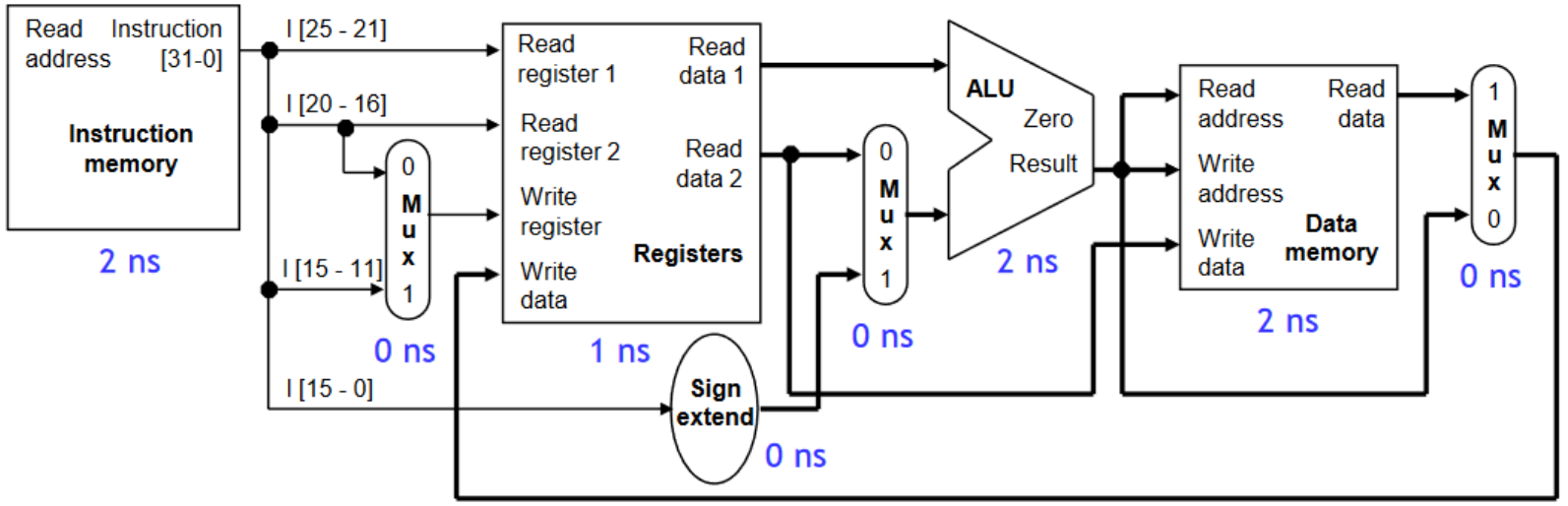
- For example, lw $t0, -4($sp) needs 8ns, assuming the delays shown here.

reading the instruction memory	2ns	8ns
reading the base register $sp	1ns	
computing memory address $sp-4	2ns	
reading the data memory	2ns	
storing data back to $t0	1ns	

one clock cycle: 2ns

Processor frequency: 500MHz

Cycle per Instruction (CPI) ~ 4



Single/multi-cycle (COVID19 vaccine schedule)

Single cycle (Worst case)

One shot will take 60 minutes one slot = 60 minutes

Multi cycle (average case kinda)

One shot: five to 60 minutes one slot = 15 minutes

Can We Have Both?

Faster clock rate (say 500MHz) and also CPI=1?

Dhonnobad