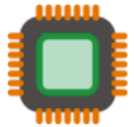


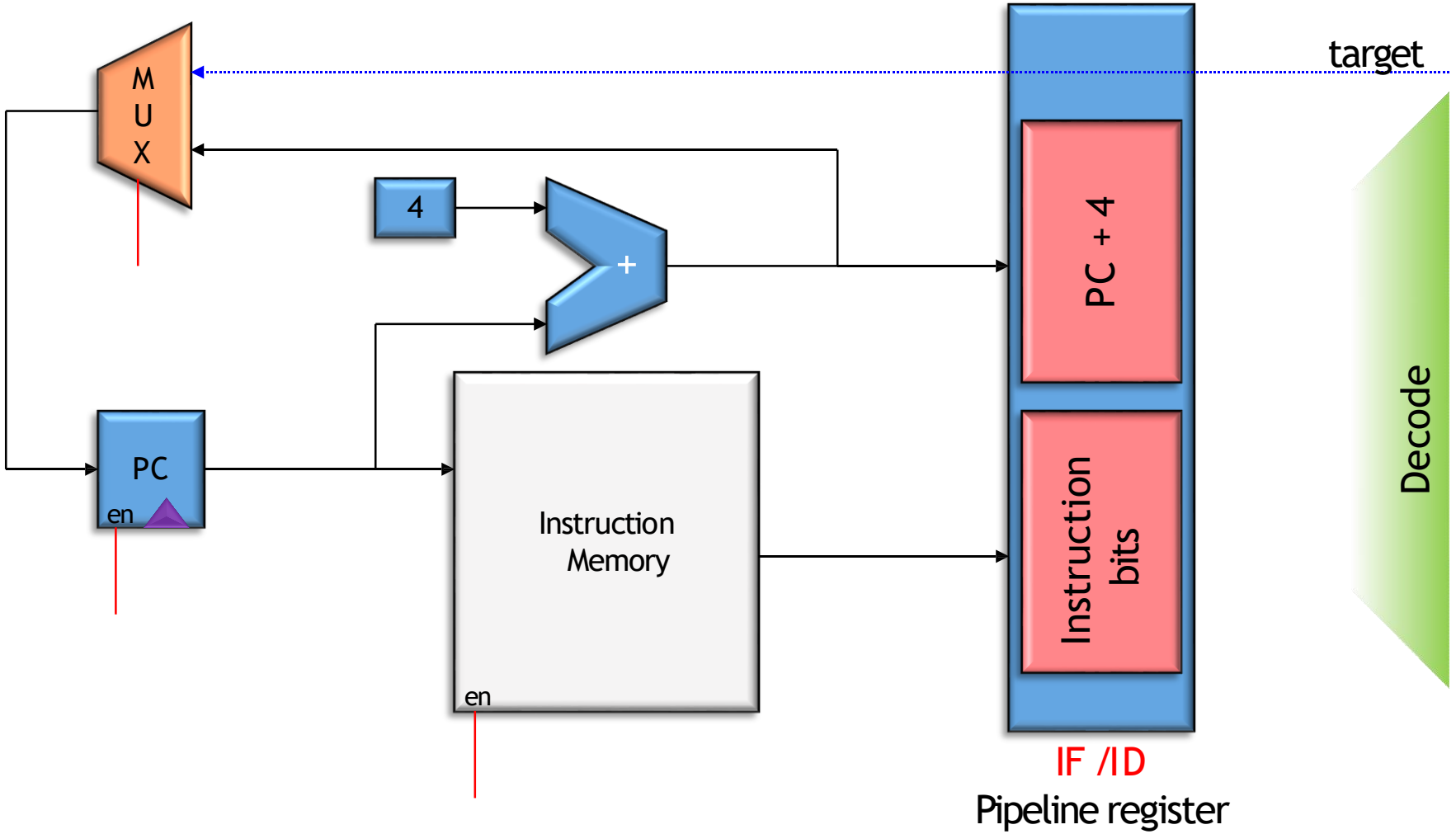
CS305: Computer Architecture

Instruction Pipelining-III

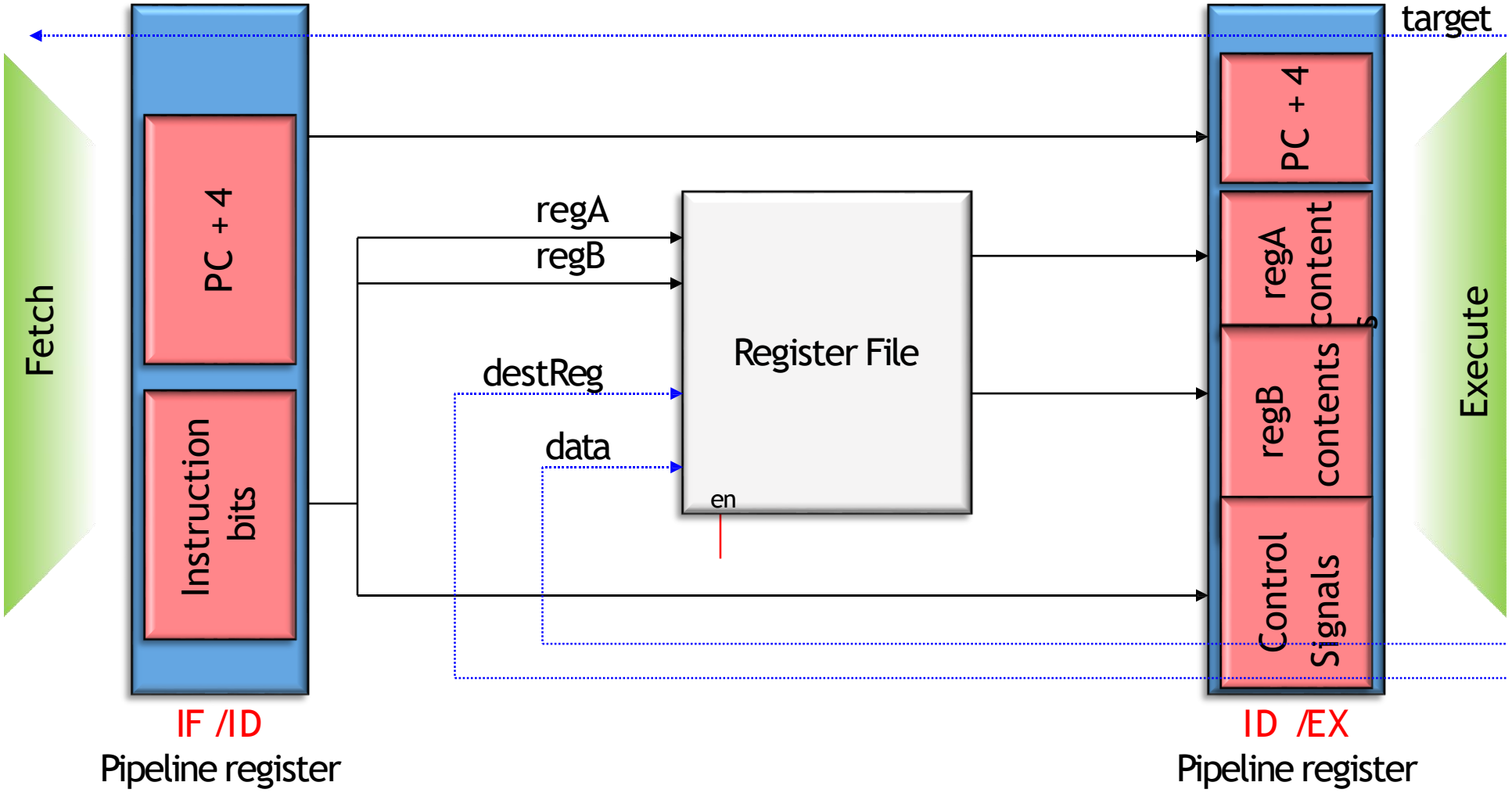
https://www.cse.iitb.ac.in/~biswa/courses/CS305/main.html

https://www.cse.iitb.ac.in/~biswa/

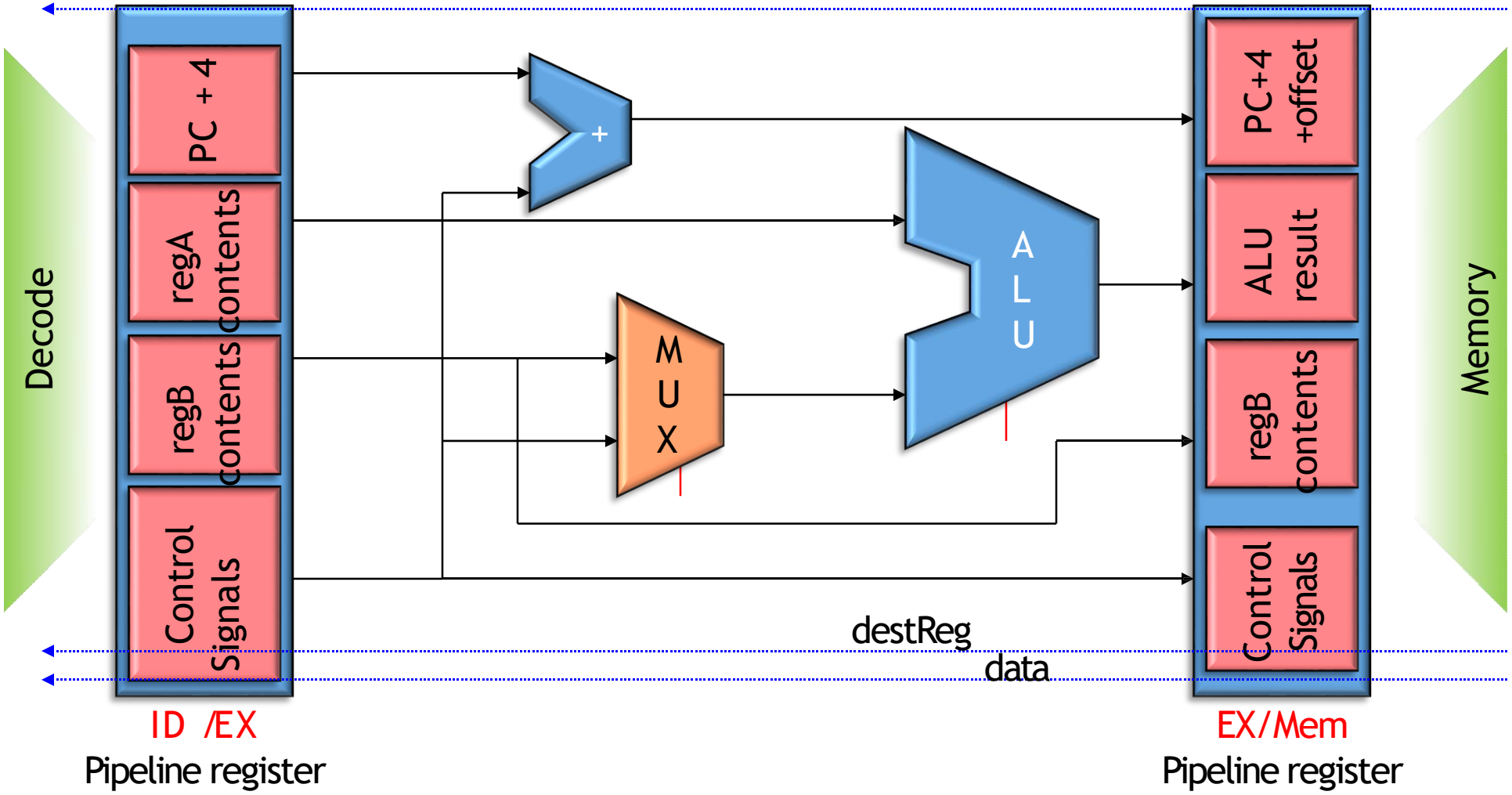
Stage-1: Fetch



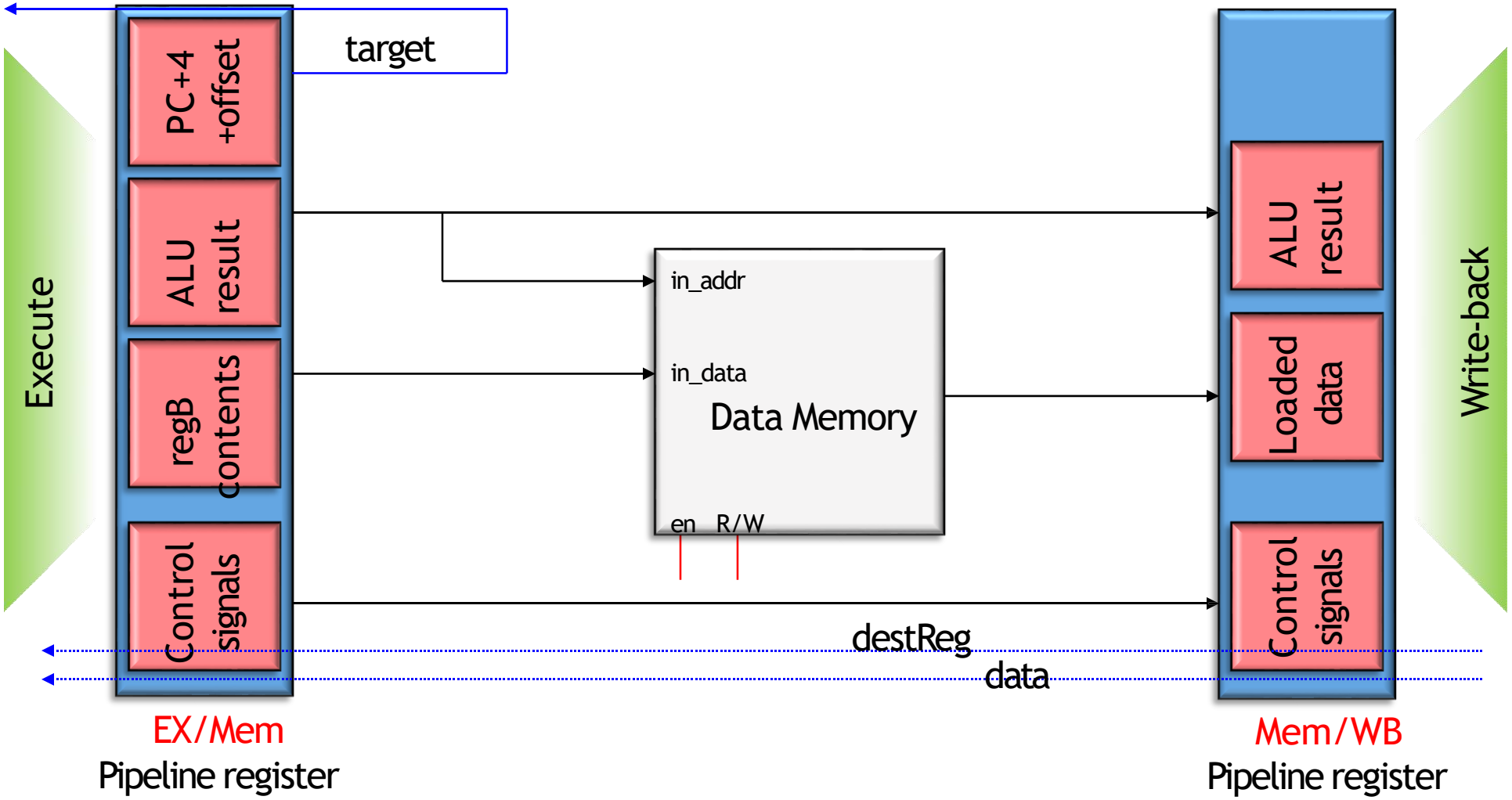
Stage 2: Decode



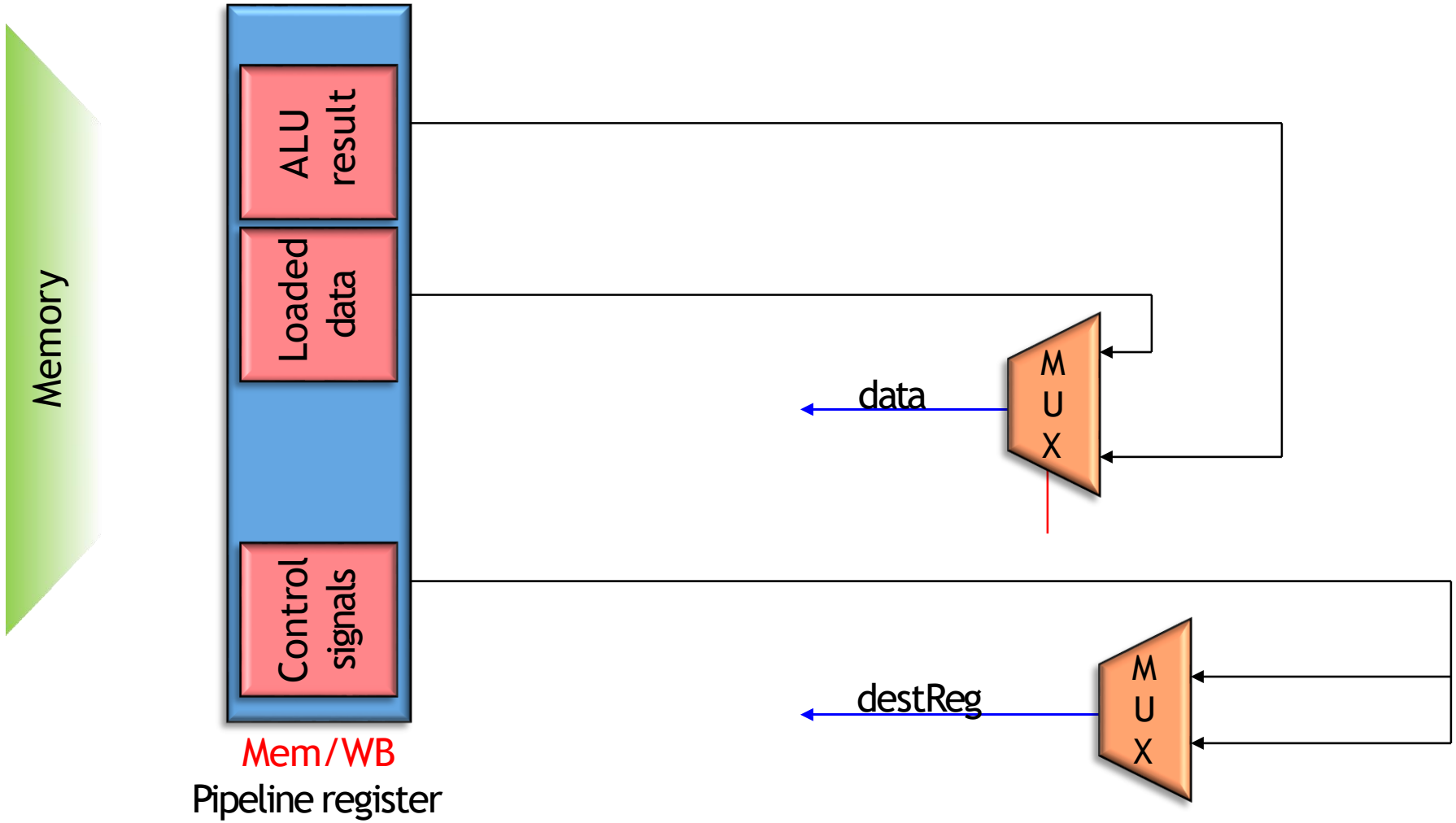
Stage 3: Execute



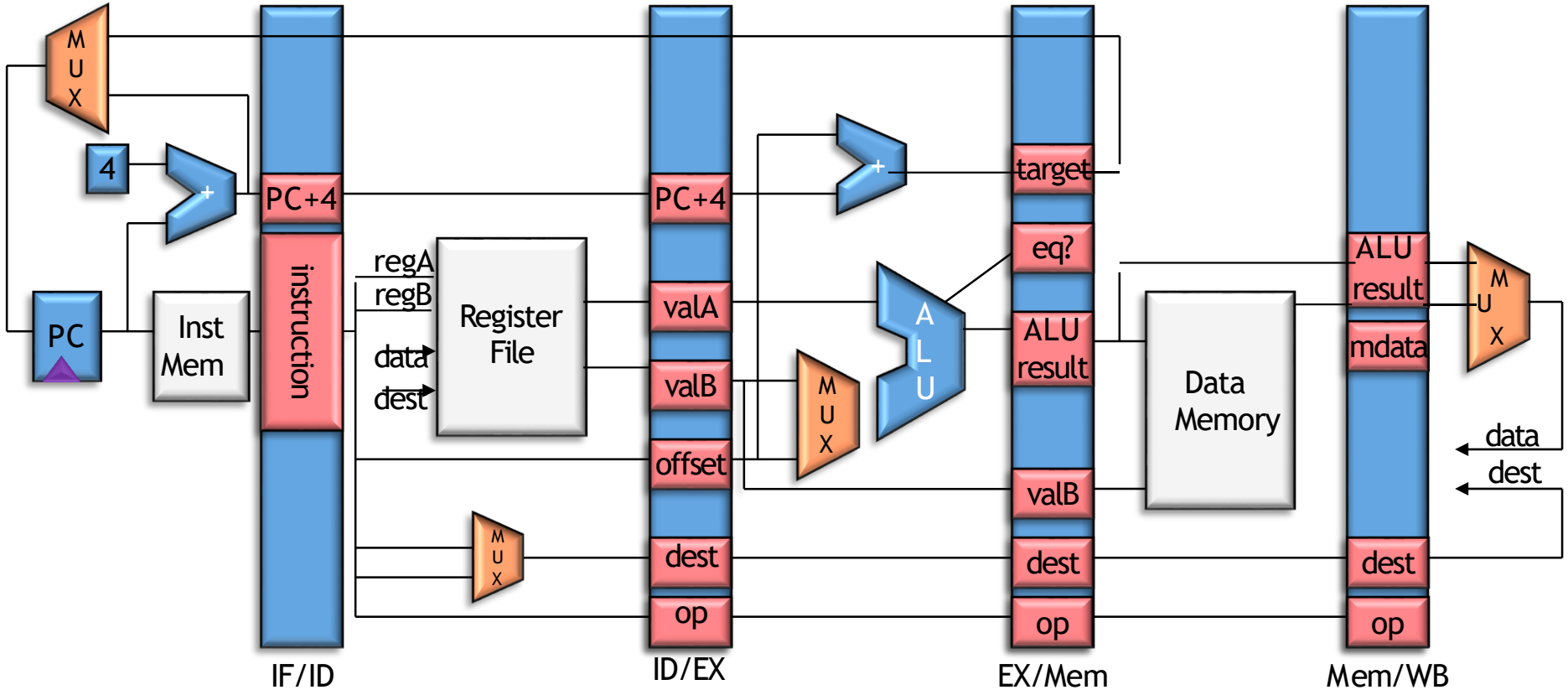
Stage 4: Memory Stage



Stage 5: Write-back



The Complete Picture



Control Signals

Control signals per stage

Refer Figure 4.50 (page no 303 of P&H)

Pipelined registers written every clock cycle too, no need of a control signal.

The ideal world

- Uniform Sub-operations
  - Operation (op) can be partitioned into uniform-latency sub-ops
- Repetition of Identical Operations
  - Same ops performed on many different inputs
- Independent Operations
  - All ops are mutually independent

The real world

- Uniform Sub-operations NO
  - –Operation can be partitioned into uniform-latency sub-ops
- Repetition of Identical Operations NO
  - –Same ops performed on many different inputs
- Independent Operations NO
  - –All ops are mutually independent

Teşekkürler