



CS305: Computer Architecture Superscalar and out-of-order processors: 10K feet view

https://www.cse.iitb.ac.in/~biswa/courses/CS305/main.html

https://www.cse.iitb.ac.in/~biswa/

Beyond Scalar

- Scalar pipeline limited to CPI \geq 1.0
 - Can never run more than 1 insn per cycle
- "Superscalar" can achieve CPI ≤ 1.0 (i.e., IPC ≥ 1.0)
 - <u>Superscalar</u> means executing multiple insns in parallel

Instruction Level Parallelism (ILP)

- Scalar pipeline (baseline)
 - Instruction overlap parallelism = D
 - Peak IPC = 1.0





Superscalar Processor

- Superscalar (pipelined) Execution
 - Instruction parallelism = D x N
 - Peak IPC = N per cycle



4

What is the deal?

We get an IPC boost if the number of instructions fetched in one cycle are independent ⁽³⁾

Complicates datapaths, multi-ported structures, complicates exception handling

Out of order (03) processor: 01 001 001 Pursuit of even higher IPC

0101 0000

110000101110001000 1000010111000100001000

Out-of-order follows data-flow order

Example:

(1) $r1 \leftarrow r4 / r7$ (2) $r8 \leftarrow r1 + r2$ (3) $r5 \leftarrow r5 + 1$ (4) $r6 \leftarrow r6 - r3$ (5) $r4 \leftarrow r5 + r6$ (6) $r7 \leftarrow r8 * r4$ /* assume division takes 20 cycles */

In-order execution

1	2	3	4	5	6
---	---	---	---	---	---

In-order (2-way superscalar)

1	2	4	5	6
	3			

Data Flow Graph

Out-of-order execution

 1

 3
 5
 2
 6

4

Two or more instructions can execute in any order if they have no dependences (RAW, WAW, WAR)

Completely orthogonal to superscalar/pipelining

O3 + Superscalar



In-order Instruction Fetch (Multiple fetch in one cycle)

O3 + Superscalar



In-order Instruction Fetch Out-of-order execution (Multiple fetch in one cycle)

O3 + Superscalar



In-order Instruction Fetch Out-of-order execution (Multiple fetch in one cycle)

In-order Commit



The notion of Commit

After commit, the results of a committed instruction is visible to the programmer

and

the order at which instructions are fetched is also visible.

Why we need in-order commit?

Think about exceptions and precise exceptions

We should know till when we are done as per the programmer's view.

Tatenda