
CASPER

# CS305: Computer Architecture

## DRAM Organization

https://www.cse.iitb.ac.in/~biswa/courses/CS305/main.html

*https://www.cse.iitb.ac.in/~biswa/*

# DRAM Organization

Channel

DIMM

Rank

Chip

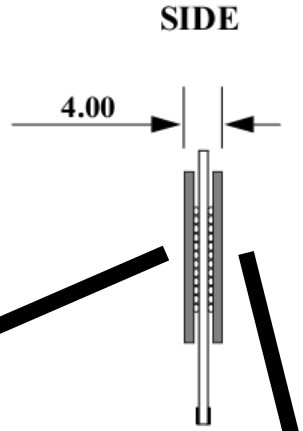
Bank

Row

Column

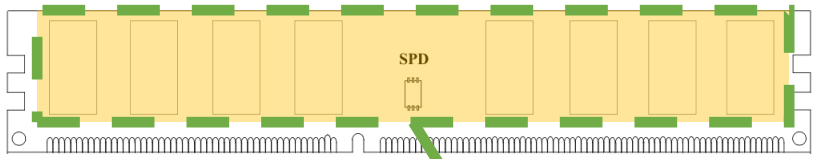
# Rank

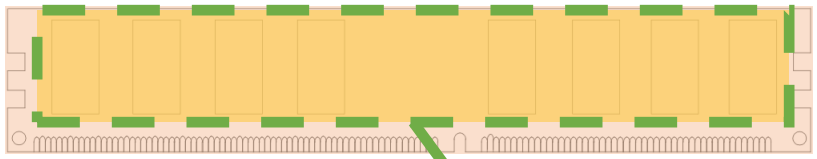
**DIMM (Dual in-line memory module)**




**Front of DIMM**

**Back of DIMM**

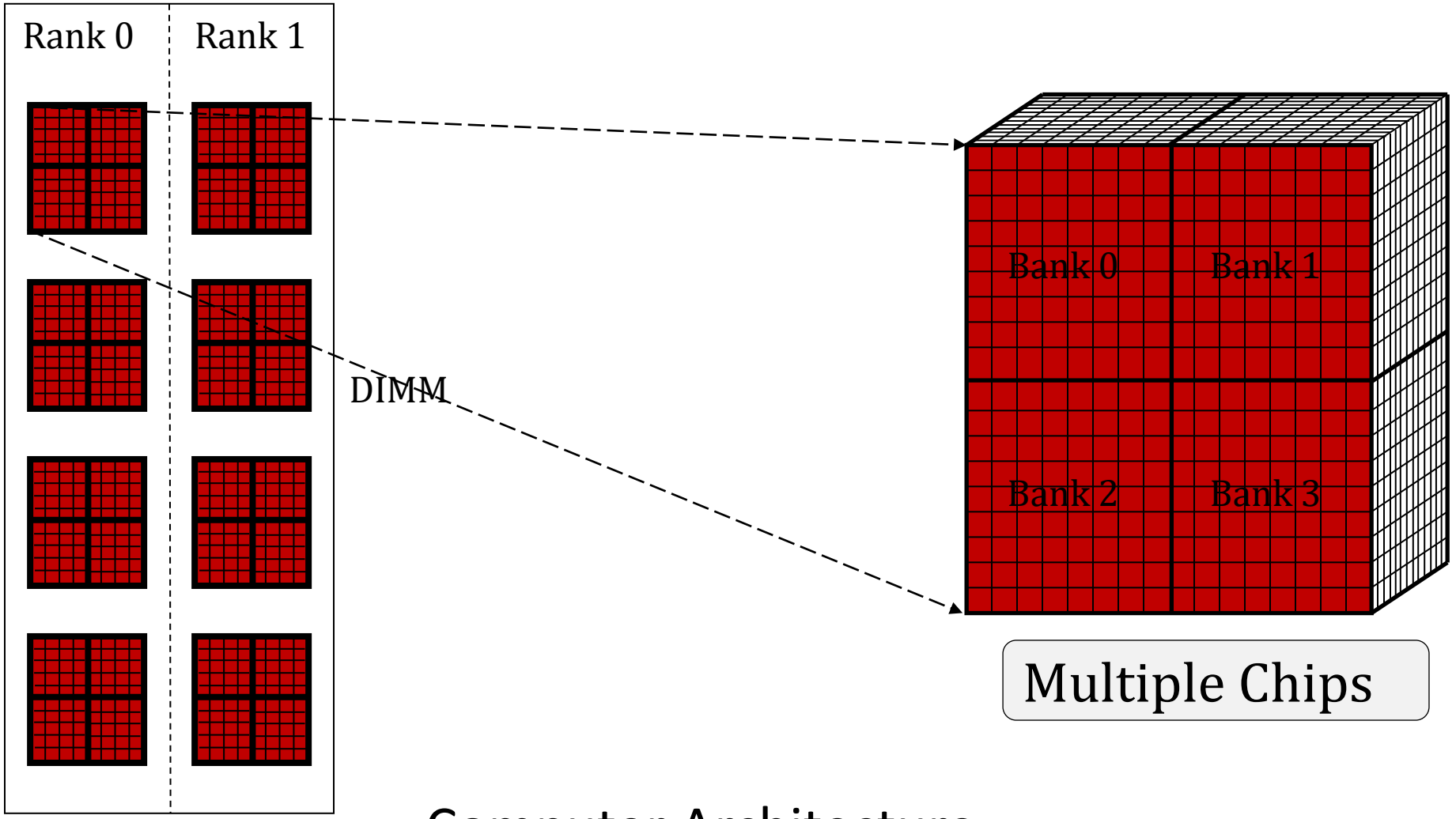


**Rank 0:** collection of 8 chips

**Rank 1**

# Ranks, Banks, Rows, Columns



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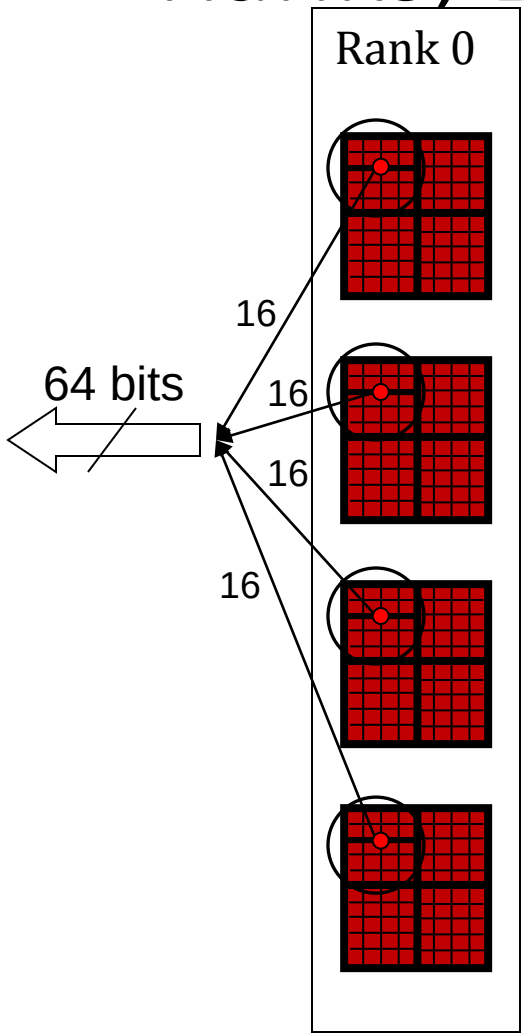
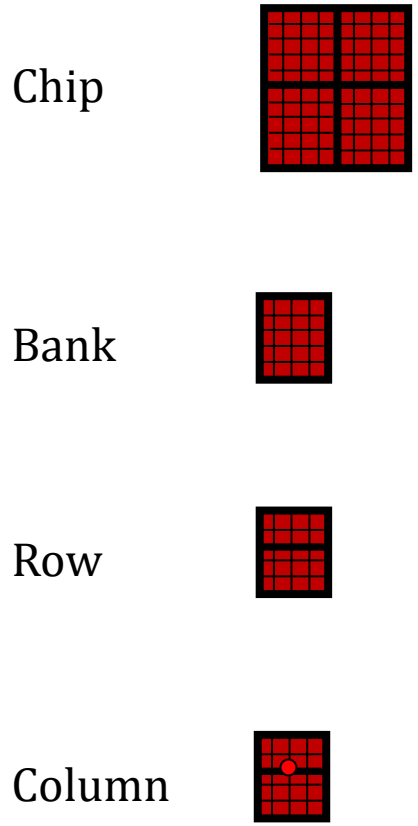
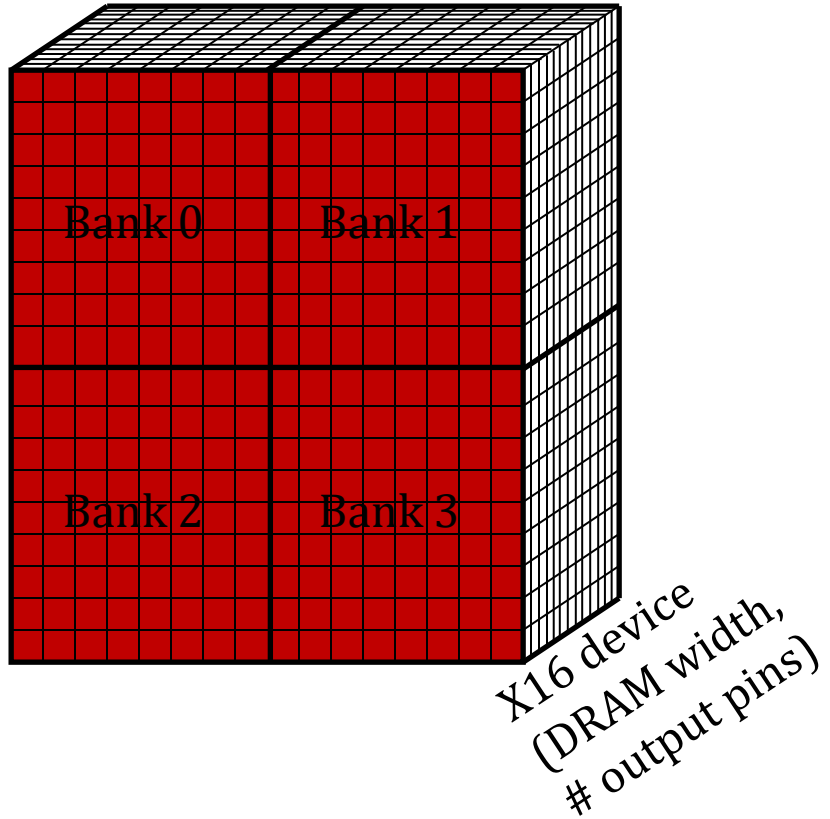



16-bit interface: 16 bits from each chip in one go

# Ranks, Banks, Rows, Columns

Each rank has 64-bit wide data bus

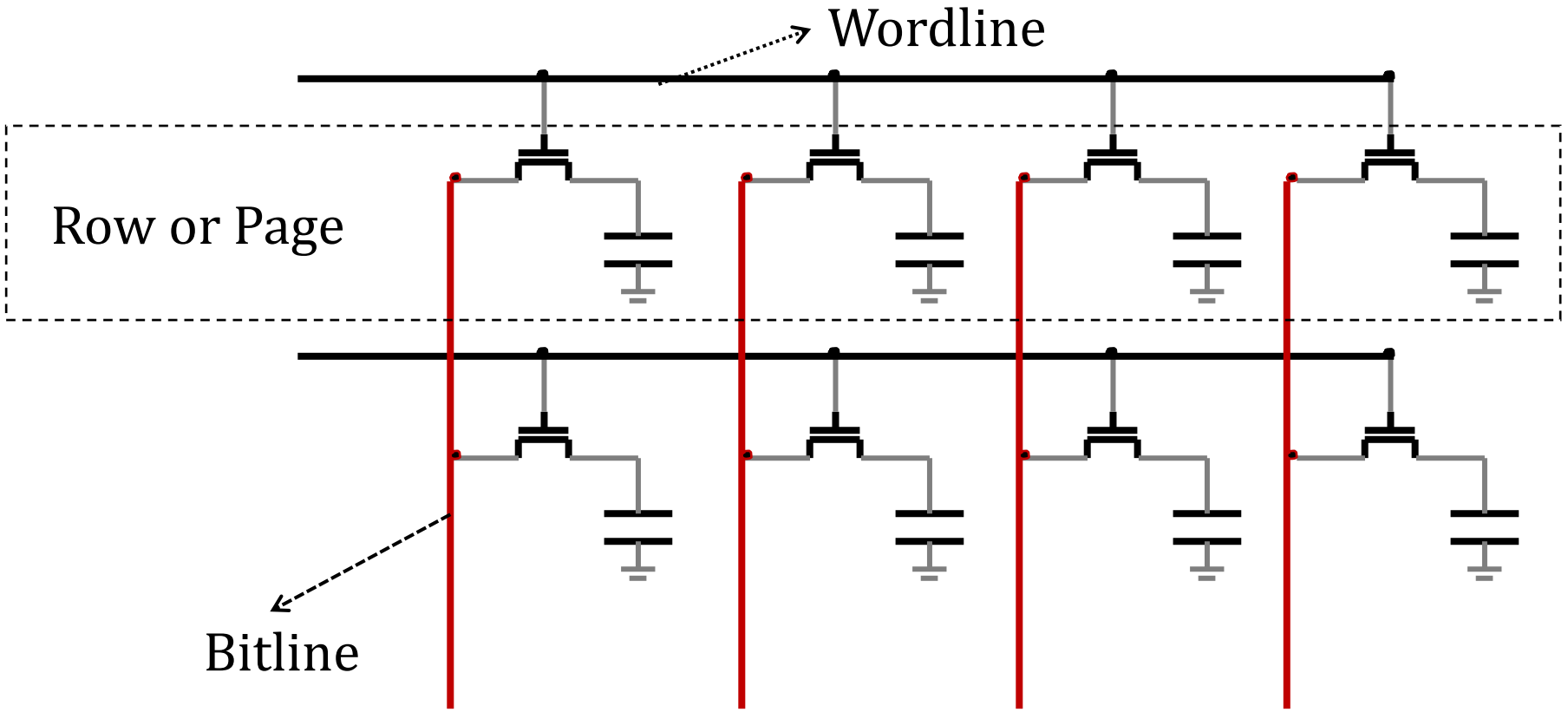
If a rank is of width x8 then # DRAM chips ??

What about x4, # DRAM chips ??

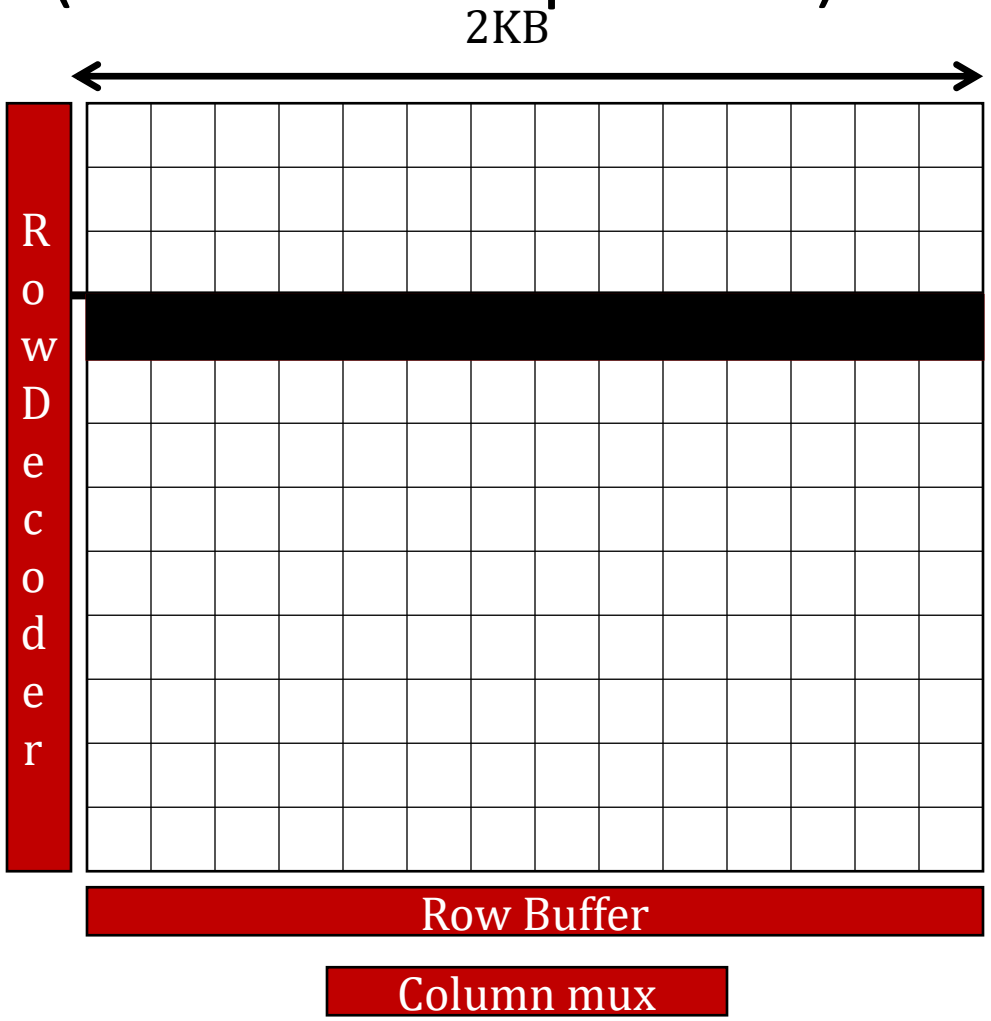
If a rank is of width x8 then # DRAM chips ?? 8

What about x4, # DRAM chips ?? 16

# The One bit, Where is it?



# Row Decoder and Row buffer (Sense Amplifier)




- Each bank has a row buffer
- Stores the last used row

# An Example

2Gb * 8 DRAM Chips (one side of the rank)

Total 16 chips + 2 chips for ECC (for both the ranks)

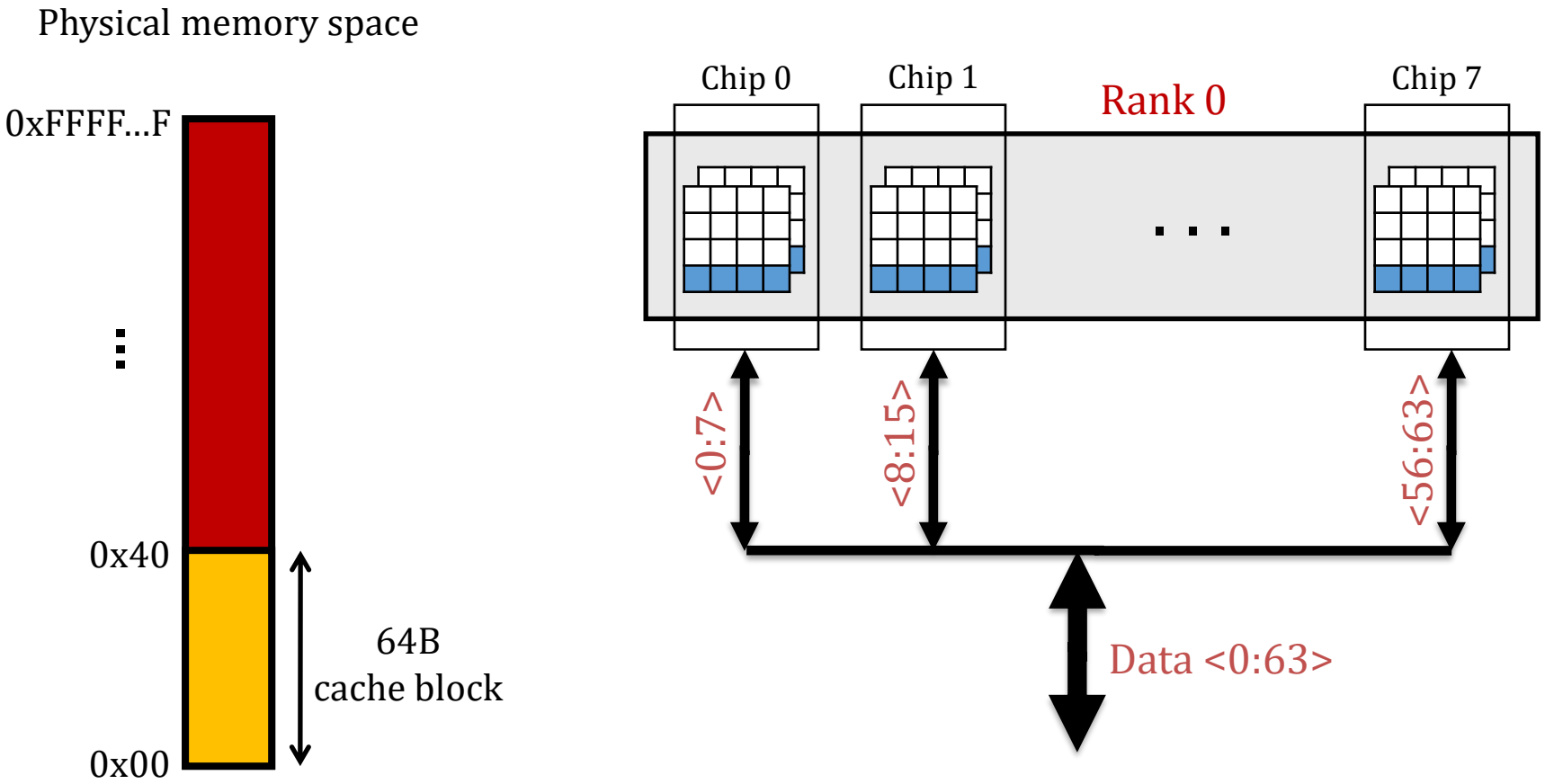
64 bit + 8 bit ECC interface (72 bit wide DIMM)

Transferring a 64B cache line will take 8 transfers of 8B each

8B will come from 8 chips (8 bits from one chip)

1 bit from each DRAM array assuming 8 DRAM arrays per bank

# DRAM to LLC interaction



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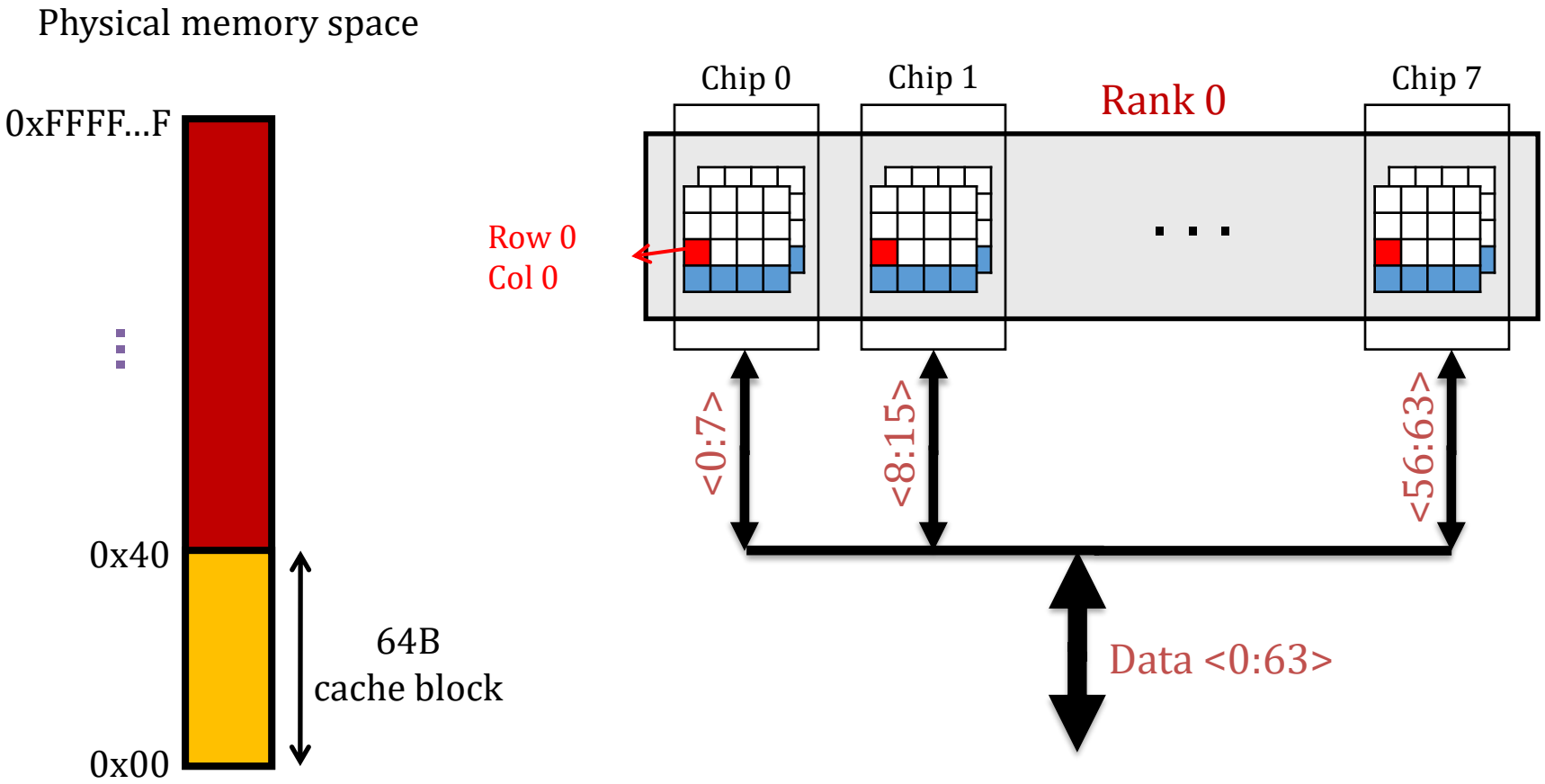

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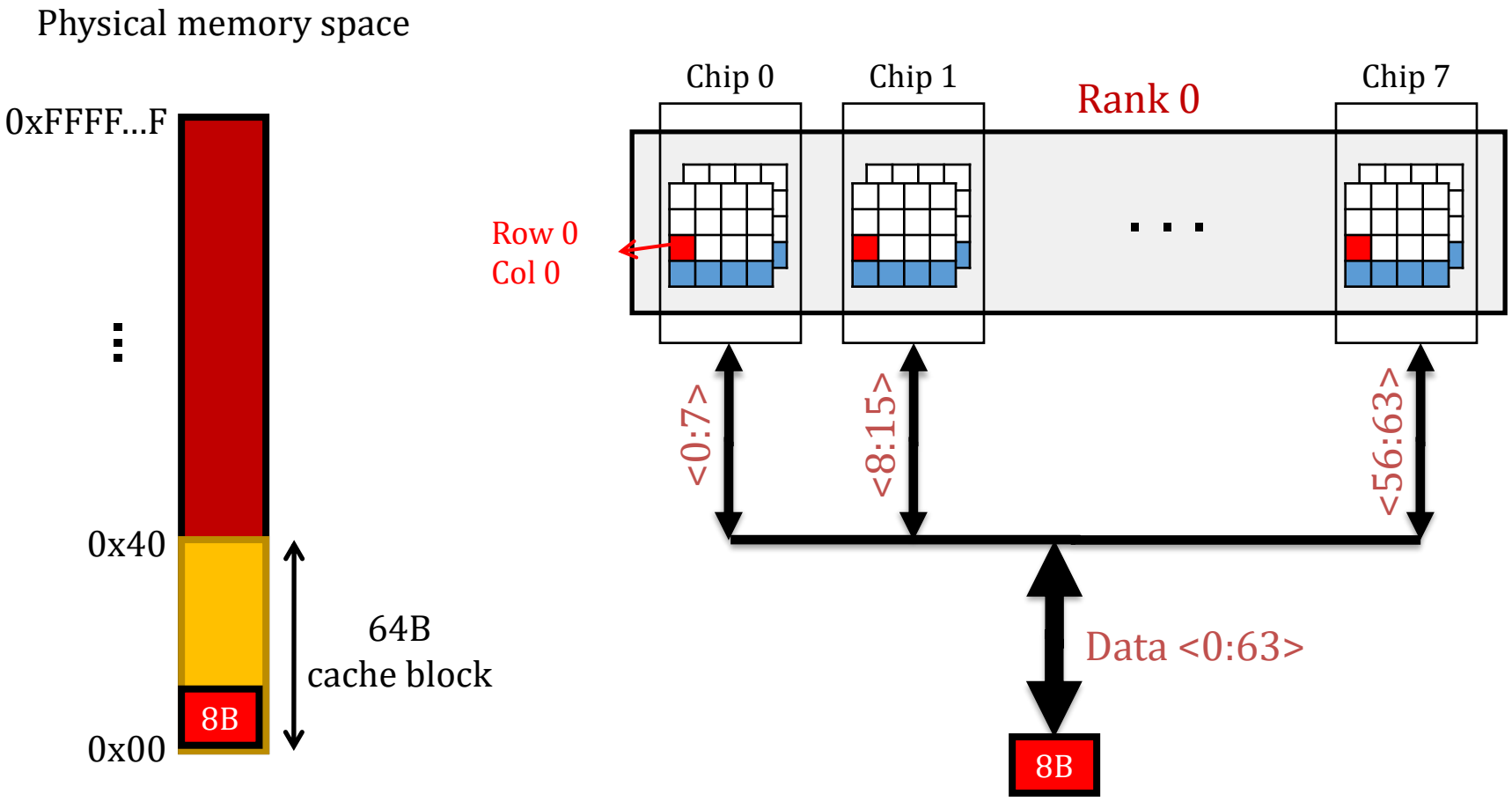
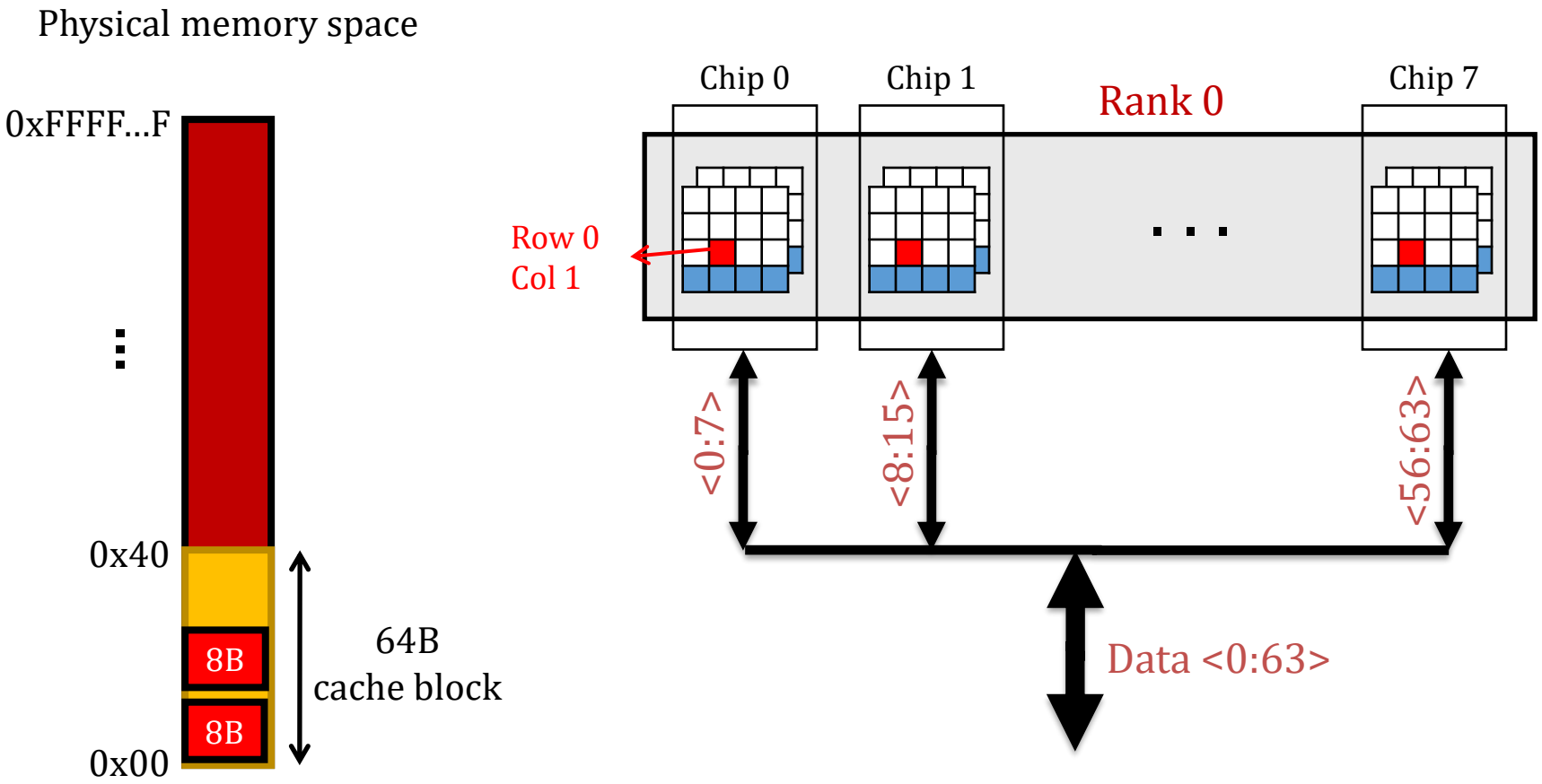


# DRAM to LLC

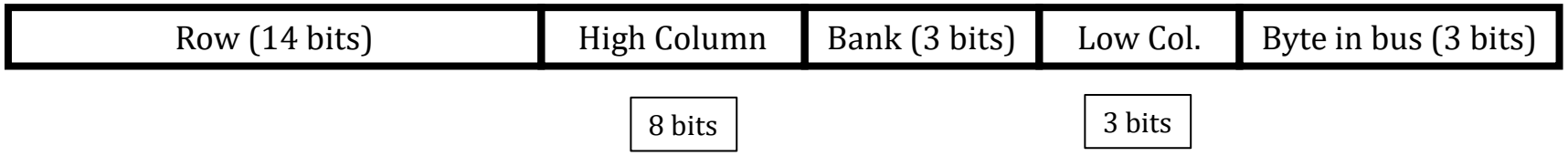



8 cycles (DRAM IO): 1 cycle transfers 8 bytes from a column

# DRAM Address Mapping (One Channel)

2GB DRAM, 8 Banks, 16K rows, 2K Columns per bank

Cache Interleaving: Consecutive cache blocks in consecutive banks




Row Interleaving: Consecutive rows in consecutive banks


What about Multiple Channels?

# Think About it

Ro Ra Ba Ch Co

Ro Ra Ba Co Ch

Ro Co Ra Ba Ch

Pros and Cons

# teşekkür ederim