## CS-341 Assignment 3

### Pipelining

### Deadline: September 27th 5 pm, Monday

### 1. 5 Stage, without forwarding or hazard detection: 5 marks

In this mode, write a sequence of instructions to show the importance of hazard detection (i.e, your code should give incorrect results when run in this mode). Add appropriate screenshots from Ripes and explain the behaviour. Also mention what hazard is causing this behaviour.

- 2. 5 Stage, without forwarding, with hazard detection: 5 marks (2.5 for each part) For both parts, add appropriate screenshots from Ripes, explanations and mention the hazard causing the behaviour,
  - a. Write a sequence of instructions that would give stalls without forwarding (in this mode) and would give no stalls when forwarding (and hazard detection) is enabled.
  - b. Write a sequence of instructions in which stalls, in this mode, can be avoided by rearranging the instructions (rearranging should not change the program logic i.e., final values in the registers)

### 3. Stalls and Forwarding: 10 marks (2 for each part)

Consider the following set of instructions.

li t0 2 li t1 10 add t0 t0 t1 li t2 5 add t2 t0 t2 li a7 1 add a0 t2 x0 ecall

Considering the processor to be a 5-stage RISC-V processor. What is the value present in the datapath connecting

- a) Address input of data memory and EX/MEM pipeline after 4th cycle assuming the processor detects hazards and has forwarding.
- b) R2 idx input of registers block and decoder after 10th cycle assuming the processor detects hazards and has no forwarding.
- c) Assuming the processor to be a 6-stage dual-issue processor, what is the value stored in opcode\_exec\_out datapath (it is present between IDII and IIEX search for it :) ) after 4 cycles.
- Provide screenshots of pipeline diagrams of all the 3 types of processors given in a,b,c and write the number of cycles needed for each type of processor.

e) Assuming the processor to be a 5-stage processor without hazard detection, what is the output of the code, what is the reason for this output and how can we overcome this problem and get the correct output.

# Please don't write changing the processor as the solution for part e (if at all there's a problem). I expect you to change the code.

### 4. Maximising Efficiency: (5 marks)

Write a code that takes 10 integers as input and gives its sum as output. When you run the code using a 5-stage processor without a forwarding unit (with hazard detection), it should consume a minimum number of clock cycles and the number of registers. First, minimise the number of clock cycles and then minimise the number of registers without compromising the number of clock cycles. Run the code in ripes and add a screenshot of the number of cycles consumed and mention the number of cycles and number of registers used in the report separately.

**Note**: The number of integers taken is fixed (10) and all 10 numbers are positive integers say 1 to 100, not more and code should be in RISC V architecture.

# Please take input using the li command. Hardcode the 10 integers but please take them differently.

### You need to print the output.

Please make sure that the code works even when I change the inputs.

### **Submission Instructions:**

You need to submit two files <roll\_no>\_A3.pdf and <roll\_no>\_A3.s. The report should contain the following things:

### For Question 1

Code, one screenshot showing that it doesn't work without hazard detection and one screenshot showing that it works perfectly when hazard detection is present. And a small explanation for what asked in the question

### For Question 2

For part a, code, one screenshot showing stalls (pipeline diagram) and one screenshot (pipeline diagram) showing that it works perfectly when the forwarding unit is present.

For part b, code, one screenshot showing stalls (pipeline diagram), then rearranged code and one more screenshot (pipeline diagram) without stalls.

### **For Question 3**

For parts a,b,c write the value and a screenshot with the cursor hovering the datapath and showing the value. Part d is clear in the question and for part e write the output and provide a screenshot for the output and write the solution and again a screenshot of the solution.

### For Question 4

Mention the minimum number of cycles consumed and the number of registers used and a screenshot of the pipeline diagram for an example. And the code for this question should be submitted as <roll\_no>\_A3.s

Create a directory with name <roll\_no>\_A3 and add these two files <roll\_no>\_A3.pdf and <roll\_no>\_A3.s and submit the zip file <roll\_no>\_A3.zip

Example:

180050017\_A3.zip

|----- 180050017\_A3

|----- 180050017\_A3.pdf |----- 180050017\_A3.s