



CS773: Computer Architecture for Performance and Security

Lecture 7: 10K Feet View on the Power-efficient Architecture

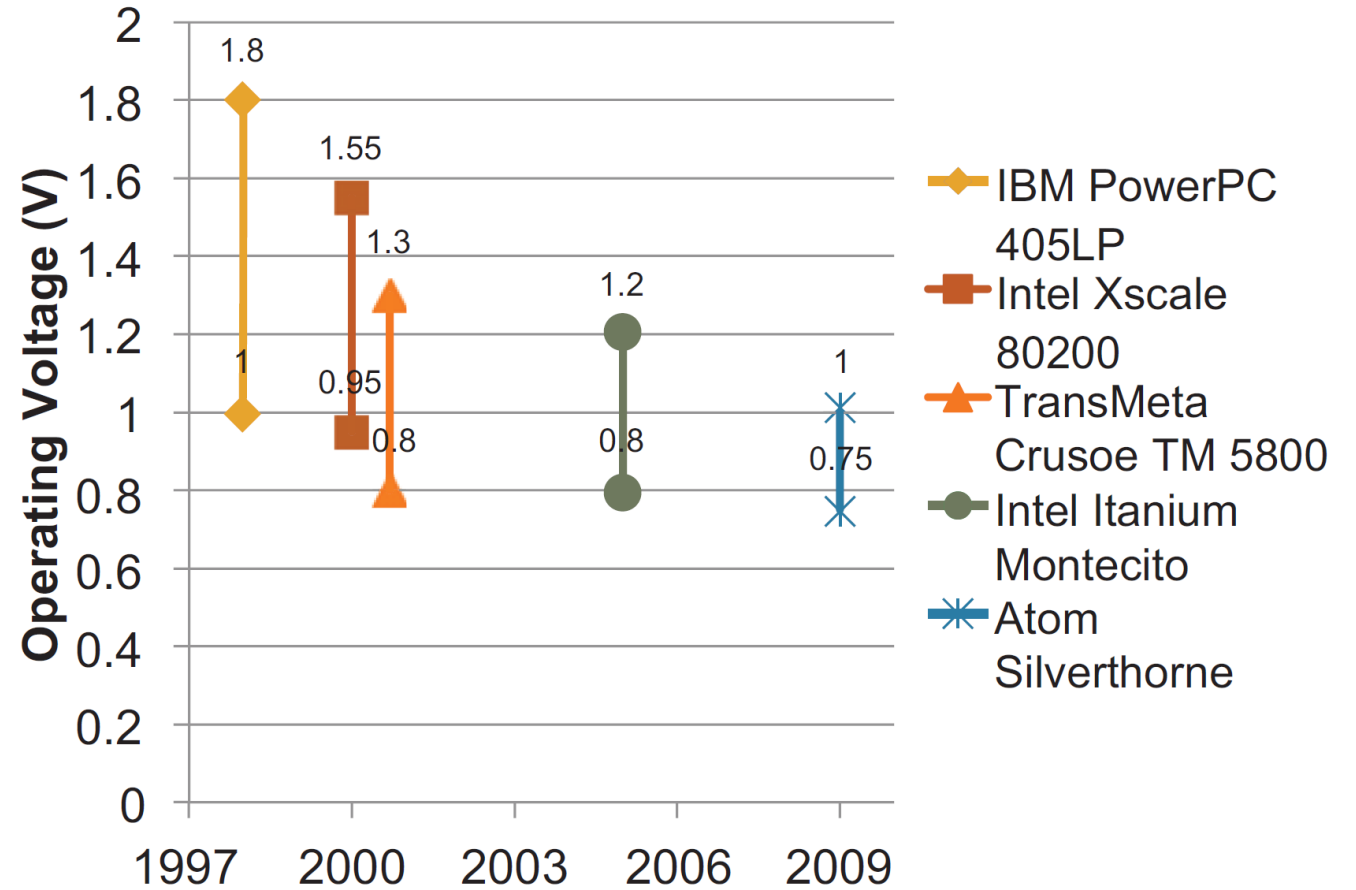
Power

Dynamic: CV^2f (frequency is also dependent on the voltage)

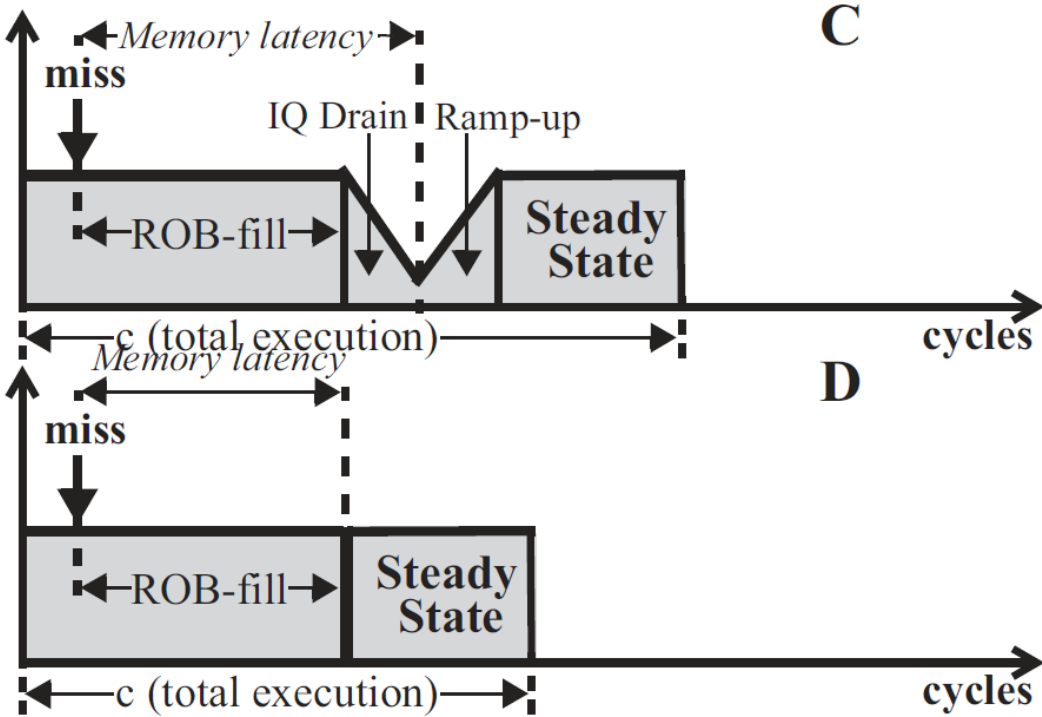
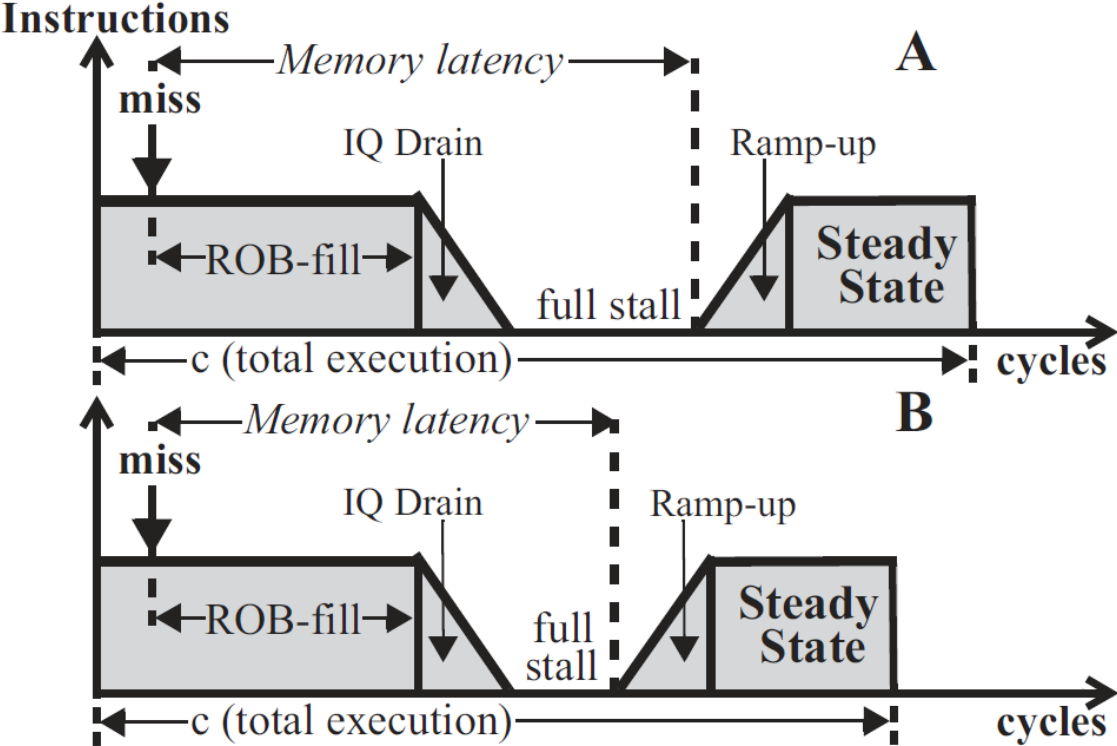
high frequency will also demand high voltage

Static: Leakage power

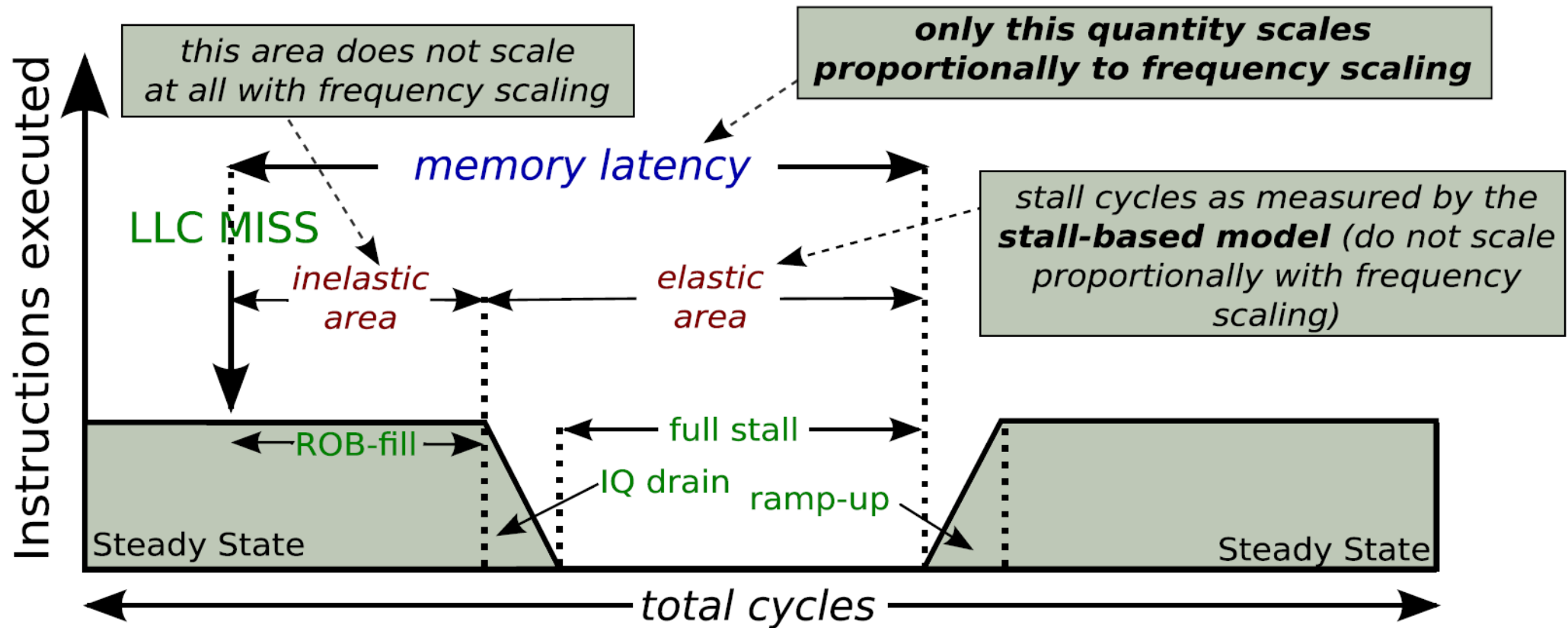
Dynamic Power



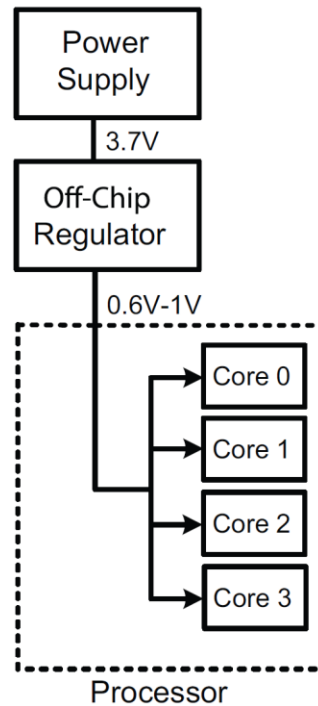
Effect of Frequency



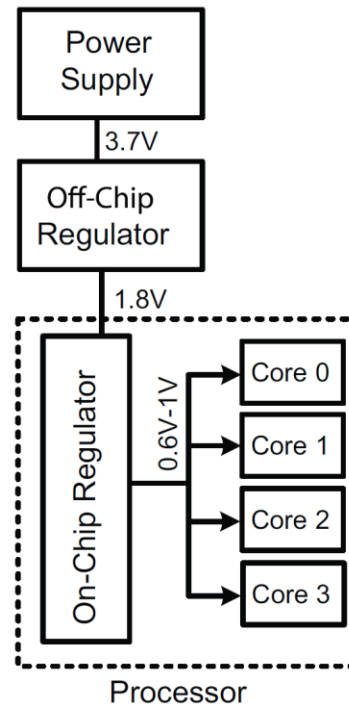
A bit Deeper



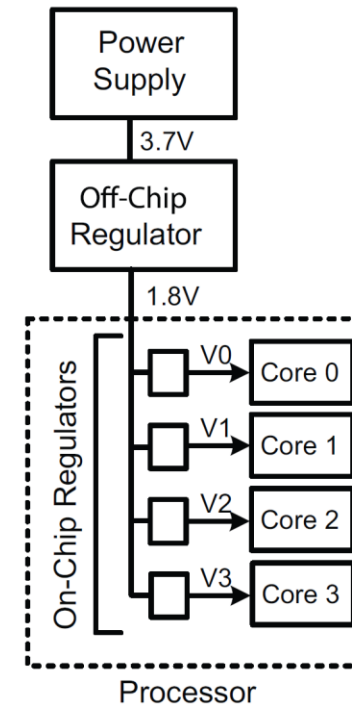
DVS (Dynamic Voltage Scaling)



No On-Chip Regulator



One On-Chip Regulator with Global DVFS



Four On-Chip Regulators with per-Core DVFS

DFS Governors

Linux: cpufreq component
(`/sys/devices/system/cpu/`): Performance, Powersave, Ondemand, Conservative, and Interactive

Hardware-managed P states (performance states)

Performance scaling ~ Frequency scaling

Per-core P states (PCPS)

Static Power (Decay Cache)

Put k-ways into the sleep mode when memory activity is low (power gating). Decay Cache, State-destroying

Example: 8MB 16-way cache becomes 512kB 2-way (intel IvyBridge)

Static Power (Drowsy Mode)

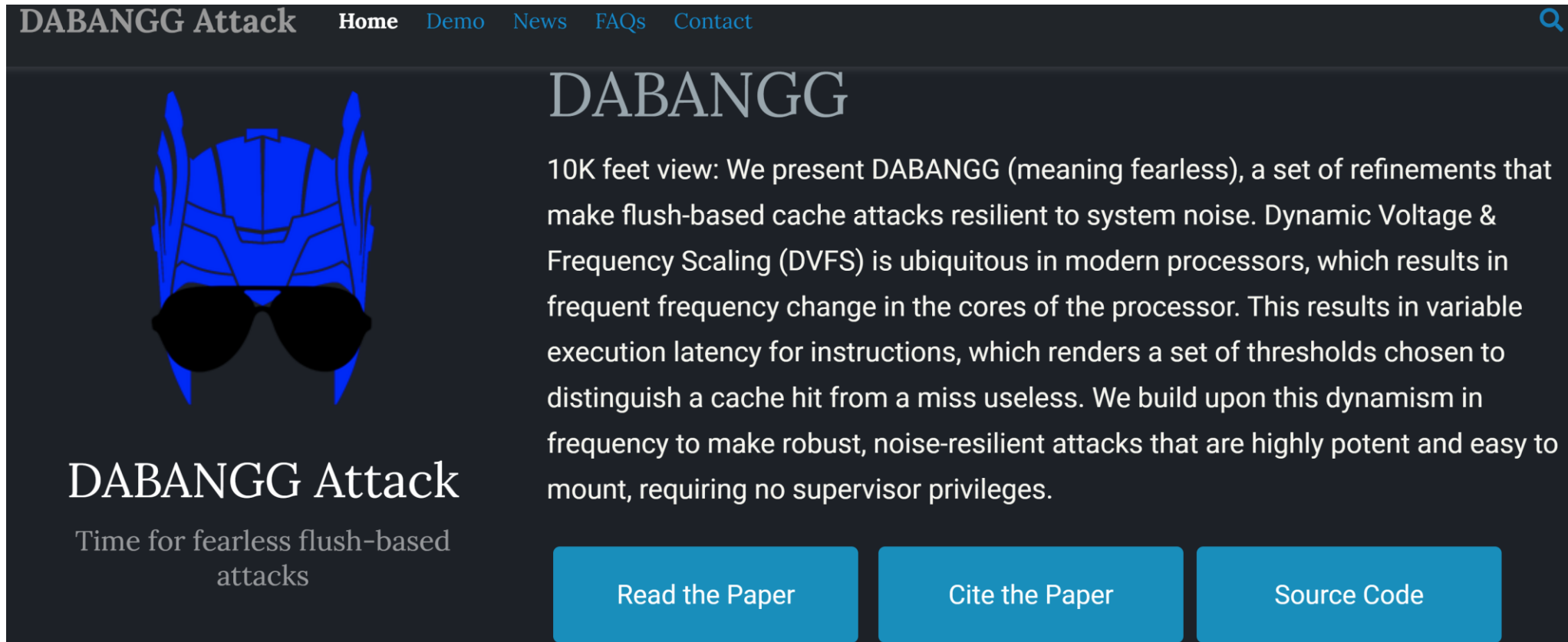
Drowsy mode: cache lines into low-power mode (line retains the data but can't access it 😊, drowsy-bit per cache line), State-preserving

Switched to normal mode: If cache line accessed again

DVFS and Security

More papers in the coming weeks

DVFS and Cache Attacks



The screenshot shows the homepage of the DABANGG Attack project. At the top, there is a navigation bar with links for Home, Demo, News, FAQs, and Contact. The main content area features a blue helmet icon with sunglasses on the left. To the right, the title 'DABANGG' is displayed in a large, serif font. Below the title, a paragraph describes the project: '10K feet view: We present DABANGG (meaning fearless), a set of refinements that make flush-based cache attacks resilient to system noise. Dynamic Voltage & Frequency Scaling (DVFS) is ubiquitous in modern processors, which results in frequent frequency change in the cores of the processor. This results in variable execution latency for instructions, which renders a set of thresholds chosen to distinguish a cache hit from a miss useless. We build upon this dynamism in frequency to make robust, noise-resilient attacks that are highly potent and easy to mount, requiring no supervisor privileges.' At the bottom of the main content area, there are three blue buttons: 'Read the Paper', 'Cite the Paper', and 'Source Code'. Below the helmet icon, the text 'DABANGG Attack' is written in a large, serif font, followed by the tagline 'Time for fearless flush-based attacks' in a smaller, sans-serif font.

DABANGG Attack

Time for fearless flush-based attacks

DABANGG

10K feet view: We present DABANGG (meaning fearless), a set of refinements that make flush-based cache attacks resilient to system noise. Dynamic Voltage & Frequency Scaling (DVFS) is ubiquitous in modern processors, which results in frequent frequency change in the cores of the processor. This results in variable execution latency for instructions, which renders a set of thresholds chosen to distinguish a cache hit from a miss useless. We build upon this dynamism in frequency to make robust, noise-resilient attacks that are highly potent and easy to mount, requiring no supervisor privileges.

Read the Paper

Cite the Paper

Source Code

To appear in WOOT 2022

<https://www.cse.iitb.ac.in/~biswa/DABANGG.pdf>

Performance and Power



Delay = runtime



Energy = Watts * runtime



EDP (Energy Delay Product) = Watts *
runtime * runtime



ED²P and ED³P



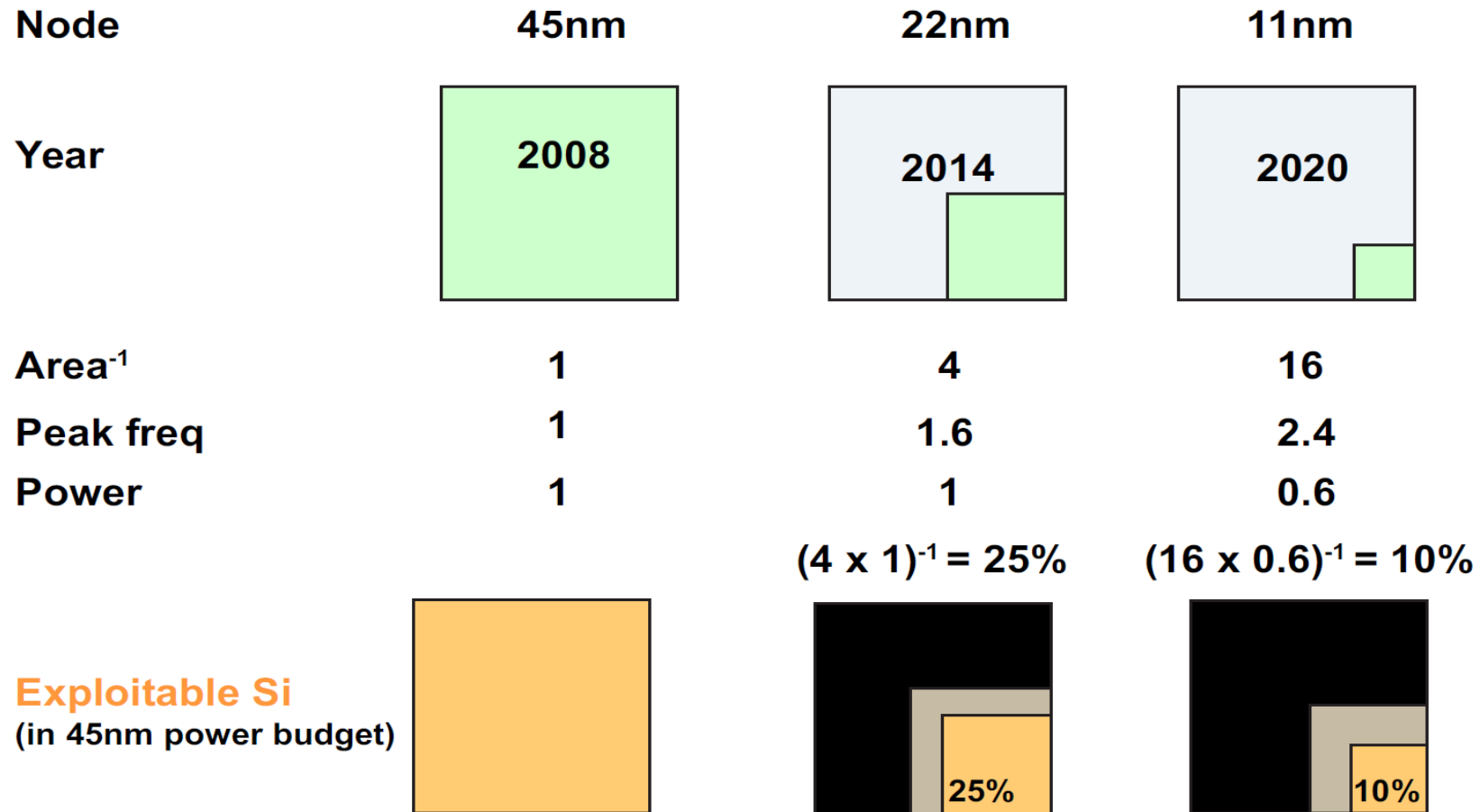
Dark Silicon



Dark Silicon

- Due to the breakdown of Dennardian scaling, the percentage of a silicon chip that can switch at full frequency is dropping exponentially with each process generation (45nm to 22nm to 11nm); larger fractions of a chip's transistors become dark. RIP Multi-core systems ☹️

Dark Silicon (End of Dennard Scaling)



Source = ITRS 2008



Why did it happen? Piazza +1

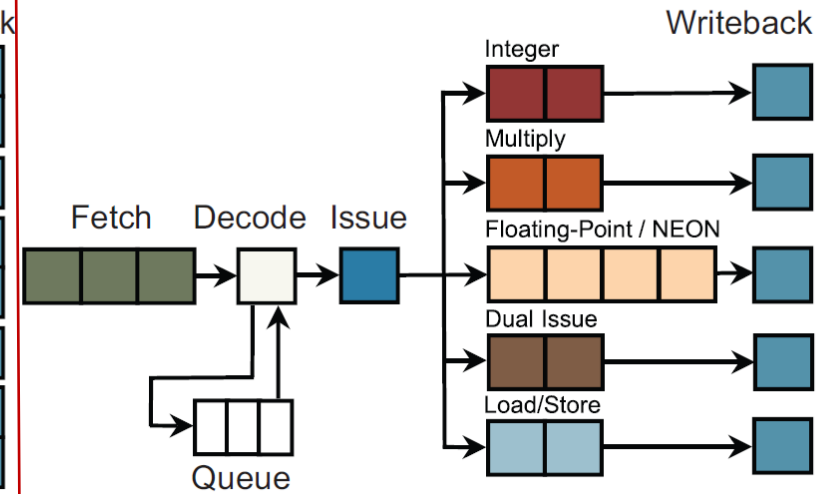
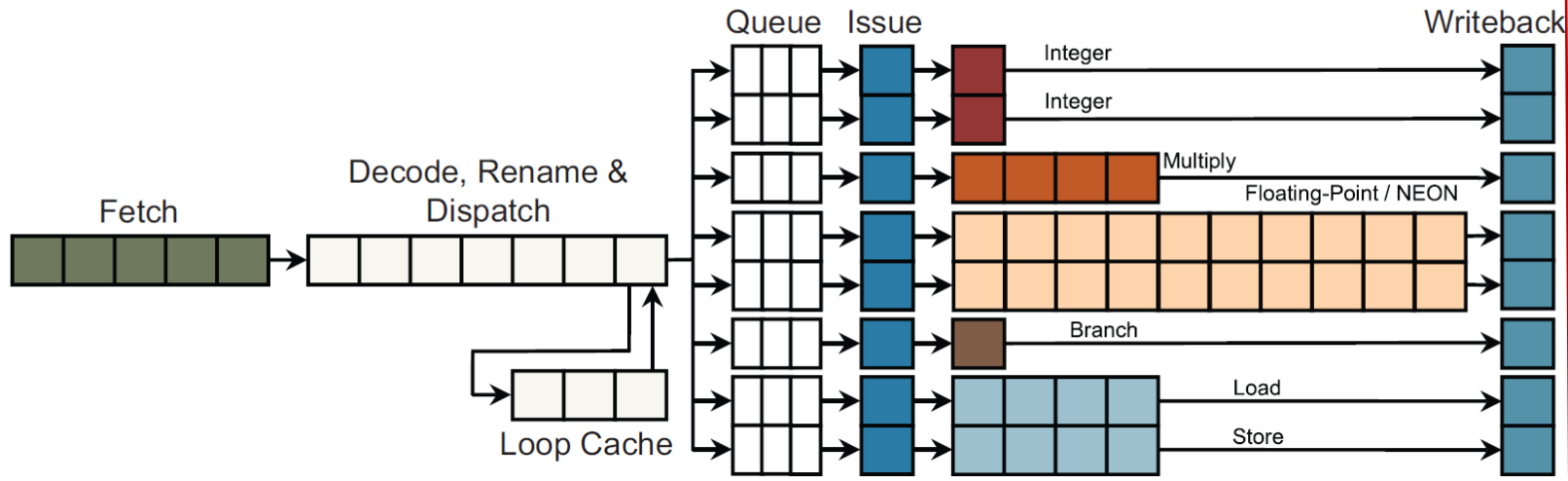


One more Wall
(Utilization Wall)

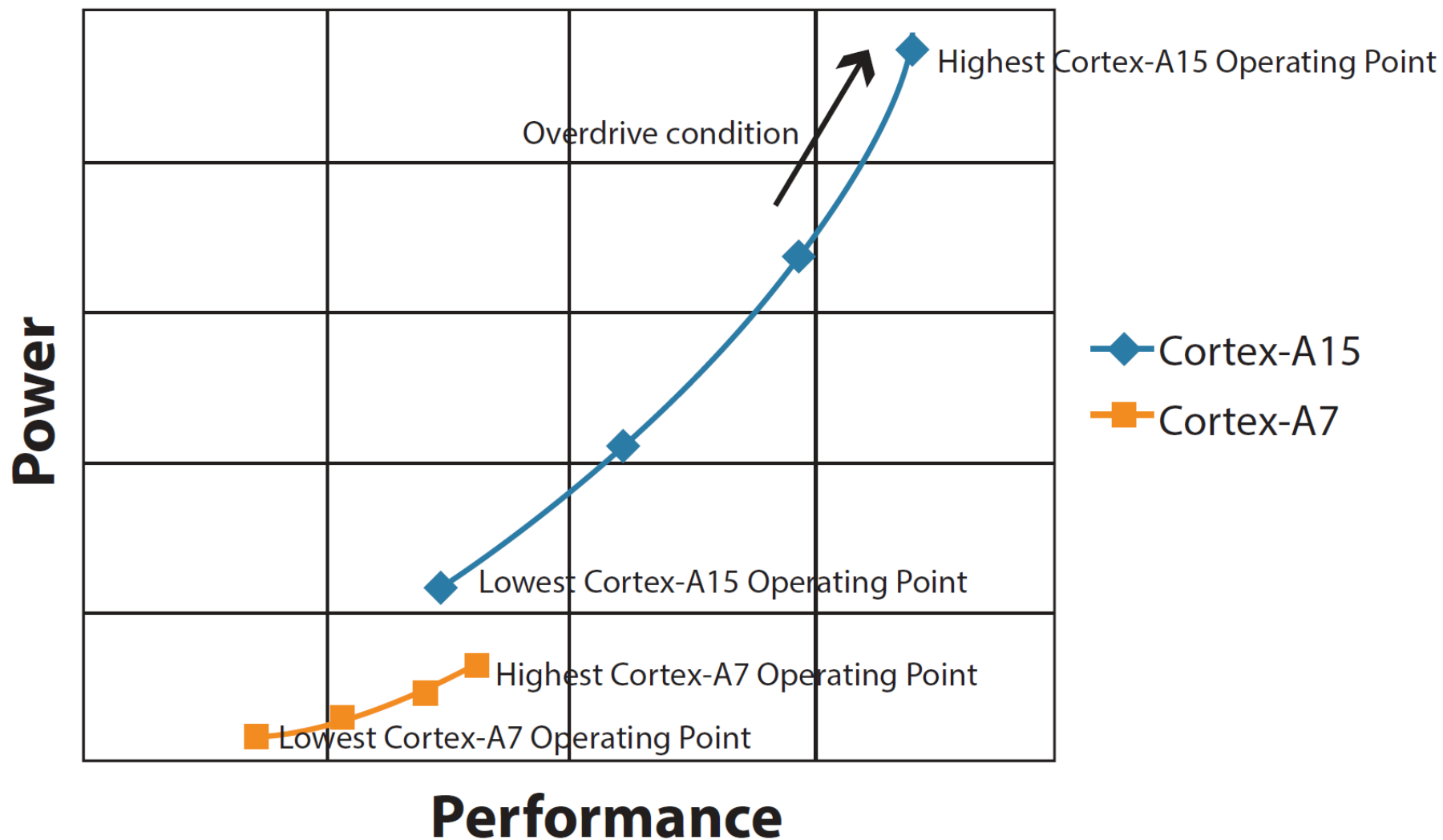
Power budgets may lead to scenarios where few (less than 20%) of the chip's transistors can be ON at a time.

The world of Single-ISA heterogeneous cores

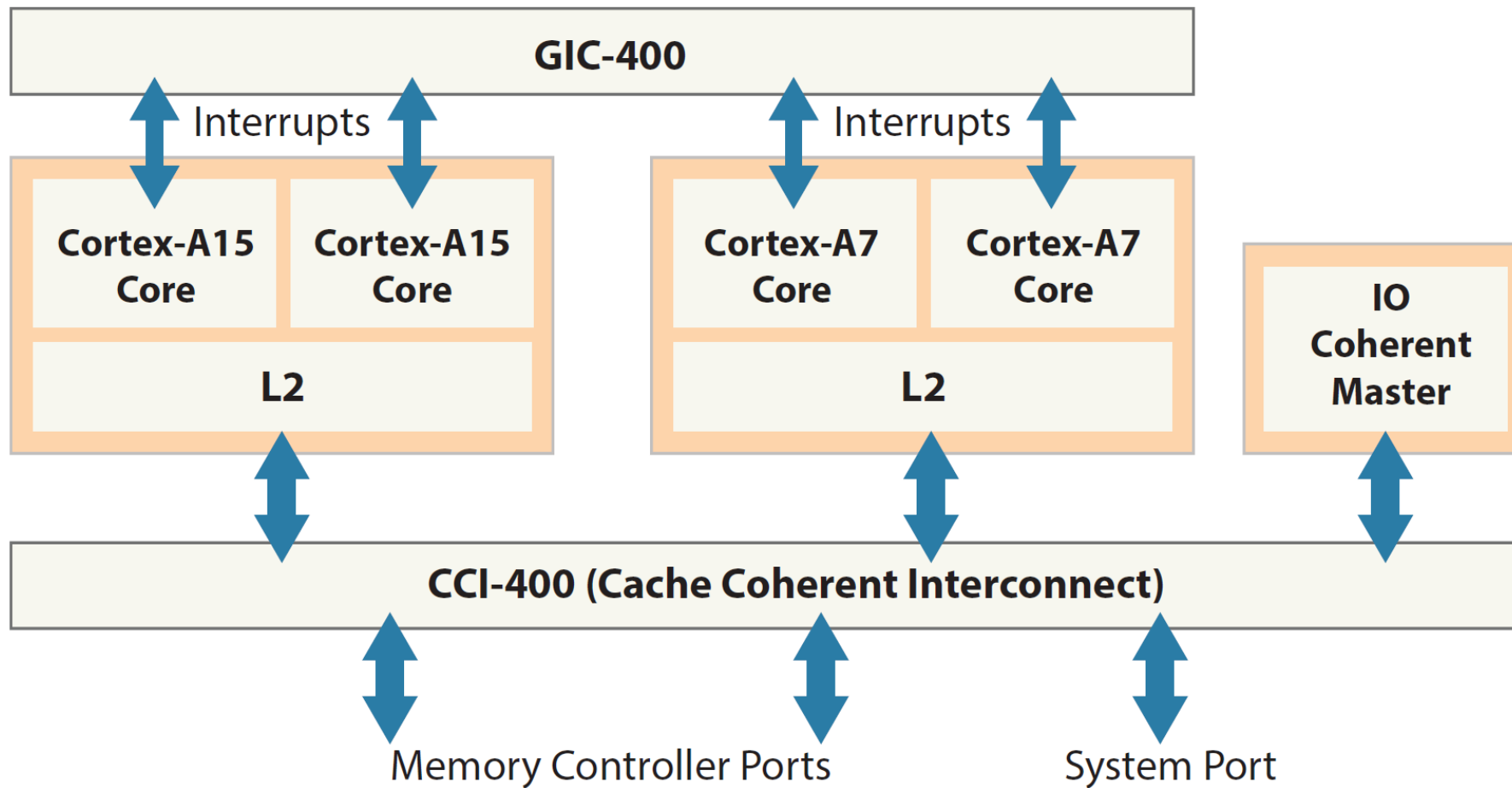
ARM Big/Little



Power/Performance Tradeoff



Big/Little Multicore (Based on P-state)



Thermal/Co2 emission ☹️

Some other day!

Thanks