Introduction to the PCI Interface

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Talk layout

- BUS standards
- PCI Local Bus
- PCI protocol
- Special Cases
- Electrical and Mechanical Specifications
- Other Topics
Inside a Computer

- What is a BUS?
  - Components – Processor, Memory etc
  - Peripherals
  - Interconnection

- Motivation
  - Data flow
  - Speed
Local Bus

- A set of parallel conductors, which allow devices attached to it to communicate with the CPU.
- The bus consists of three main parts:
  - Control lines, Address lines, Data lines

![Diagram showing how devices are attached to a generic bus.]

<table>
<thead>
<tr>
<th>Key</th>
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<tbody>
<tr>
<td>Data Lines</td>
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<tr>
<td>Address lines</td>
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<tr>
<td>Control lines</td>
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BUS Protocols

- Requirements of a BUS standard
  - Electrical, Mechanical requirements
  - Protocol requirements

- Common BUS standards
  - ISA and EISA
  - MCA (Micro Channel Bus)
  - VESA Local BUS (Video Electronic Standard Associations) – 1-2 devices can be connected.
  - PCI Local BUS
ISA (Industry Std Arch.)

- Has a clock speed limit of 8 MHz
- Has a word length of 8 or 16 bits (8 or 16 data lines)
- Requires two clock ticks to transfer data (16 bit transfers)
- Very slow for high performance disk accesses and high performance video cards
EISA (Enhanced Std Arch)

- Has a clock speed of 8.33 MHz
- Maximum of a 32-bit wide word length (32 data lines)
- Can support lots of devices
- Supports older devices which have Slower or Smaller word lengths (ISA)
- Transfers data every clock tick.
MCA (Micro-channel Bus)

- Has a clock speed of 10 MHz
- Has a 32 bit word length (32 data lines)
- Transfers data every clock tick.
VESA (Video Electronic Std Arch.)

- Has a clock speed limit of 33 MHz.
- Limited to a 32-Bit wide word length (32 data lines).
- Cannot take advantage of the Pentium’s 64 bit architecture.
- Limited support for Burst Transfers, thereby limiting the achievable throughput.
- Restricted on the number of devices which can be connected (1 or 2 devices).
PCI Local Bus

- Bus Width – 32 or 64 bits
- Operating frequency – 0-66 MHz
- Can support many more devices then VESA
- 64 bit extension for Pentium proc.
- Greater Variety of Expansion cards available.
- Multiplexed Address and Data
- PCI SIG (Special Interest Group)
PCI Local Bus Revisions

- 1.0 – 1992.
- 2.0 – connector and expansion board specification
- 2.1 – 66MHz operation
- 2.2 – protocol, electrical and mechanical specs
PCI General Block Diagram
PCI Local Bus Features

- **Performance** –
  - Burst Transfer at 528 MBps peak (64 bit- 66 MHz)
  - Fully concurrent with Processor-Memory subsystem
  - Access time is as fast as 60ns.
  - Hidden central arbitration.
- **Low cost** – multiplexed, no glue logic
- **Low Pin count** – 47 pin for target; 49 pin as initiator.
- **Ease of Use** – full auto configuration
- **Flexibility** – processor independent, accommodates other protocols
- **Green Machine** – CMOS drivers -> low power
Every device on the PCI bus is either
- PCI compliant – has the same signals as the PCI bus
- Connected via a PCI core – this piece of hardware does the interfacing

Common devices
- Audio/Video cards
- LAN cards
- SCSI controllers
PCI Interface Signals

**Required Pins**
- **Address & Data**
  - AD[31::0]
  - C/BE[3::0]#
  - PAR
- **Interface Control**
  - FRAME#
  - TRDY#
  - IRDY#
  - STOP#
  - DEVSEL#
  - IDSEL
- **Error Reporting**
  - PERR#
  - SERR#
- **Arbitration (masters only)**
  - REQ#
  - GNT#
- **System**
  - CLK
  - RST#

**Optional Pins**
- **64-Bit Extension**
  - AD[63::32]
  - C/BE[7::4]#
  - PAR64
  - REQ64#
  - ACK64#
  - LOCK#
  - INTA#
  - INTB#
  - INTC#
  - INTD#
- **JTAG (IEEE 1149.1)**
  - TDI
  - TDO
  - TCK
  - TMS
  - TRST#
PCI System Signals

- CLK: clean signal derived from the clock generator (33MHz, 66MHz)
- RST#: Active Low Asynchronous reset
- PAR: Parity Signal to ensure the parity across the AD bus and C/BE.
PCI Bus Protocol -
Signal Definition

- AD - Multiplexed address and data lines
- C/BE# - Command and Byte Enables
- FRAME# - Master indicating start/end of transfer
- IRDY# - Master (initiator) ready
- TRDY# - Target ready
- DEVSEL# - Target device selected
- REQ# - Request for bus
- GNT# - Bus Grant
PCI control signals contd.

- **STOP# [I/0]**: Target asserts to stop the transaction in Progress.
- **IDSEL [I]**: Used as chip select
- **LOCK# [I/0]**: During semaphore currently accessed target locked by initiator
- **DEVSEL# [I/0]**: Asserted by target when the target asserts has decoded its address. (if by 6 clk not asserted => master abort.)
PCI Configuration Register

- Device ID
- Vendor ID
- Status / Command reg
- Base Address [0,1,2,3,4,5]
- Maximum Latency
- Minimum GNT
- Subsystem ID, Subsystem Vendor ID
PCI Command Types [C/BE]

- 0000 -> INTR ack
- 0010 -> I/O Read
- 0011 -> I/O Write
- 0110 -> Memory Read
- 0111 -> Memory Write
- 1010 -> Configuration read
- 1011 -> Configuration write
JTAG boundary scan

- Test Access Port
  - Test Clock
  - Test Data in
  - Test Data out
  - Test Mode select
  - Test Reset
- IEEE standard 1149.1 compliant
Interrupts

- Asynchronous events
- 4 interrupt lines for multi-functional devices.
- Interrupt lines go to the interrupt controller to execute the ISR
PCI Bus Protocol – Transfer mechanism

- Configuration read/write
- IO read/write
- Burst
  - Basic form of data transfer
  - Includes one address phase
  - One or more data phase
Burst Transfer Mechanism

- Assert REQ#
- GNT# granted
- Wait for current transaction to end
- Assert FRAME#
- Transfer data when both TRDY# and IRDY# are asserted
- De-assert FRAME# during last data phase
Timing Diagram for a basic Read operation
Various read transaction

- Single cycle Read
- Burst data read
- Read with no wait states
- Byte Enables can be changed for every data cycle
- Data Cycle with NO byte enables.
Basic Write Operation
Transaction termination

- Last data phase completes when
  - !FRAME and TRDY (normal - master)
  - !FRAME and STOP (target termination)
  - !FRAME and Device Select Timer expires (Master abort)
  - !DEVSEL and STOP (Target abort)
Multiple bus

- PCI to PCI bridge
- Concept of LOCK
- All on one level
Thank you
Books for reference

- PCI System Architecture
  Tom Shanley and Don Anderson..Mindshare