# *Dhantu Buragohain*


**Contact Information**

*email:* dhantu@cse.iitb.ac.in
*website:* http://www.cse.iitb.ac.in/~dhantu/


**Research Interests** My research interests lie in the broad area of computer systems and networks.

**Education**

**Indian Institute Of Technology Bombay(IIT-B), India** — Mumbai, India
Ph.D. in Computer Science and Engineering — January 2015 -
Advisor: Prof. Mythili Vutukuru — GPA: 8.26/10

**Jorhat Engineering College, India** — Assam, India
B.Tech in Computer Science and Engineering — June 2010
BTP advisor: Dr. Sauravjyoti Sarmah — Percentage: 72.66

**Papers**

[1] **Dhantu Buragohain**, Abhishek Ghogare, Trishal Patel, Mythili Vutukuru, Purushottam Kulkarni, "DiME: A Performance Emulator for Disaggregated Memory Architectures", APSys, 2017.(link)

[2] Shounak Chakraborty, Dipika Deb, **Dhantu Buragohain** and H. K. Kapoor, "Cache capacity and its effects on power consumption for tiled chip multi-processors", International Conference on Electronics and Communication Systems(ICECS), 2014.(link)

[3] Shirshendu Das, **Dhantu Buragohain** and H. K. Kapoor, "A reduced overhead replacement policy for Chip Multiprocessors having victim retention", International Conference on Electronics and Communication Systems(ICECS), 2014.(link)

**Research Experience and Thesis**

**System softwares overhead in disaggregated memory architecture(in progress)**
*Advisor: Prof. Mythili Vutukuru*
Disaggregating memory from compute nodes poses several challenges. The major problem in this architecture comes from the fact that remote memory access latency using existing network technology can be in the order of microseconds. Since existing software systems are bad at hiding microsecond scale latencies, running unmodified application will suffer from performance penalty. One of the major contributors of this overhead is the paging and swapping subsystem. Currently, we are exploring the causes of these overheads and how to mitigate them such that application performance does not suffer in disaggregated memory architecture.

**DiME: A performance emulator for disaggregated memory architectures**
*Advisor: Prof. Mythili Vutukuru*
Resource disaggregation, and memory disaggregation, in particular, can have a significant impact on application performance, due to the increased latency in accessing a portion of the system's memory remotely. While applications need to be redesigned and optimized to work well on these new architectures, the unavailability of commodity disaggregated memory hardware makes it difficult to evaluate any such optimizations. To address this issue, in this work we developed DiME, an emulator for disaggregated memory systems. Our tool can emulate different access latencies over different parts of an application's memory image as specified by the user.

**A reduced overhead replacement policy for chip multiprocessors having victim retention**
*Supervisor: Prof. Hemangee K. Kapoor*
CMP-VR is an approach to dynamically increase the associativity of heavily used sets without increasing the cache size. It achieves this by reserving a certain number of ways in each set to be shared with other sets and the remaining are private to the set. These shared ways from all sets form common reserve storage, while the private ways form the normal storage. In this project, we implemented an optimization on CMP-VR by removing the LRU policy from the normal storage of the set. A victim from this normal storage can reside in the reserved/shared area and will get evicted from here using the LRU policy.

**Cache capacity and its effects on power consumption for tiled chip multi-processors**
*Supervisor: Prof. Hemangee K. Kapoor*
In this work we presented a study of reducing cache capacity and analyzing its effect on power and performance. We reduced the number of available cache banks and saw its effect on reduction in dynamic and static energy.

**Density based clustering of gene expression data**
*B.Tech Thesis, Supervisor: Dr. Sauravjyoti Sarmah*
Our implementation provides a way of elucidating the pattern hidden in gene expression data which provides a tremendous opportunity for an enhanced understanding of functional genomics. Density-based clustering was done using density estimation. We employed a divide and conquer principle that can extract clusters efficiently with the reduced number of comparisons.

**Teaching Experience**

TA for CS224: Computer Networks(2015), CS101: Computer Programming(2015-2016), CS347: Operating Systems(2016), CS333: Operating Systems Lab(2016) at IIT Bombay.

**Course Projects**

**Implementation of a file system** Kernel Programming
As a part of the course project, we first emulate a disk in RAM. A device driver was implemented for the disk on RAM. Then we implemented a simple file system capable of basic functionalities.

**Optimization of VM checkpoint** Topic in virtualization and cloud computing
The goal of this project was to optimize the size of the VM snapshot and the time taken for the snapshot operation. We modified the existing method of VM checkpointing by considering only the memory aspect of it. To optimize, we first identified the dirty pages by analyzing the page cache and then copied those pages to the secondary storage during the checkpoint operation.

**Operating directly on text files** Implementation techniques for relational database systems
Initialization cost in form data loading is a major bottleneck for applications with large file sizes. To avoid loading data from text files into the database application we provide a functionality where the user can directly access and query on the data files in a given format(*.csv). In this project, we took the existing PostgreSQL source code and modified it accordingly to achieve our goal.

**Skills**

*Programming Languages*: C, Python, C++, HTML.

*Libraries and Tools used*: GDB, MySQL, PostgreSQL, Wireshark, tcpdump, blktrace.

**Industry Experience**

**SIQES** Aug 10 - Feb 12

- Worked as a quality assurance analyst.
- Automated software testing using QTP and Selenium.

**Technical talks**

- Presented "DiME: A Performance Emulator for Disaggregated Memory Architectures" in APSys 2017.
- Presented "Cache capacity and its effects on power consumption for tiled chip multi-processors" in ICECS 2014.
- Presented "A reduced overhead replacement policy for Chip Multiprocessors having victim retention" in ICECS 2014.

**Scholarships**

- Awarded travel grant to attend ICECS, 2014.