Soumitra Pal

Contact Information	SIC-310, Kanwal Rekhi Building (KReSIT) Department of Computer Science and Engineering Indian Institute of Technology – Bombay Powai, Mumbai, MH 400076, India	<i>Cell:</i> +91 98697 73453 <i>Fax:</i> +91 22 2572 0022 <i>Email:</i> mitra@cse.iitb.ac.in <i>Web:</i> www.cse.iitb.ac.in/~mitra
Research Interests	Algorithms, Bioinformatics, Combinatorial Optimization, Parallel and Distributed Systems, Machine Learning	
Education	Indian Institute of Technology – Bombay, Powai, Mumbai, India	
	 Ph.D., Computer Science and Engineering Thesis: Scheduling Light-trails on WDM Paths and Rin of Graphs Advisor: Professor Abhiram G. Ranade Area of Study: Graph Theory, Approximation Algorit CPI: 9.0/10 (course work and seminar) 	
	 M.Tech., Computer Science and Engineering Thesis: <i>Improving branch-and-price algorithms for solvi</i> Advisor: Professor Abhiram G. Ranade Area of Study: Branch-And-Price based Exact Algorith CPI: 9.11/10 	
	Bengal Engineering and Science University, Shibpur, Howrah, West Bengal, India	
	B.E., Computer Science and Technology	July 2000
	 Thesis: Synthesis of Cellular Automata and Multiple Att Advisor: Professor Parimal Pal Chaudhuri Area of Study: Cellular Automata Marks: 85.2% 	ractor Cellular Automata based classification
Publications	Soumitra Pal, Ankita Mawandia, and Srinivas Aluru. "Distile: Extending Reptile for Insert Delete Errors." In preparation.	
	Soumitra Pal, and Srinivas Aluru. "In Search of Perfect Conference on Computational Advances in Bio and Medical S	
	Ajit Diwan, Soumitra Pal, and Abhiram Ranade. "Componen Split Graphs." <i>Under review in Discrete Applied Mathematic</i>	
	Vijay Arya, T. S. Jayram, Soumitra Pal, Shivkumar Kalyanara Meter Measurements in Distribution Networks." <i>e-Energy</i> ,	e ;
	Soumitra Pal, and Abhiram Ranade. "Scheduling Light-trails and Distributed Computing, 72(10):1226–1236, 2012.	s on WDM Rings." In: <i>Journal of Parallel</i>
	T. S. Jayram, Soumitra Pal, and Vijay Arya. "Recovery of a Sparse Integer Solution to an Underdeter- mined System of Linear Equations." <i>Workshop on Sparse Representation and Low-rank Approximation</i> <i>in 25th Annual Conference on Neural Information Processing Systems</i> , Granada, Spain, 12-17 December 2011.	
	Soumitra Pal, and Abhiram Ranade. "Scheduling Light-trail 17th International Conference on Advanced Computing and O India. December 2009.	
	Soumitra Pal, Ish Dham, and Tor E. Jeremiassen. "Design and Validation Techniques to Implement a Robust Hindsight Feature on ISA Simulators." In: <i>Global Signal Processing Expo and Conference –</i> <i>GSPx</i> , Santa Clara, USA. September 2004. [Unrefereed].	

Soumitra Pal, and Prem Kumar Vadapalli. "A methodology for Saving and Restoring the State of ISA simulators." In: *Global Signal Processing Expo and Conference – GSPx*, Santa Clara, USA. September 2004. [Unrefereed].

ACADEMIC Indian Institute of Technology – Bombay, Mumbai, India

Teaching Assistant

Experience

Experience

Services

- Assisted instructors in evaluating quizzes, exams, assignments and scribing lecture notes
 - CS 101: Computer Programming Utilization
 - CS 218/CS 301: Design and Analysis of Algorithms
 - CS 435: Linear Optimization
 - CS 606: Foundations of Parallel Computing

Web Administrator

• Maintained by frequently updating our *PhpWebSite* based departmental website

PROFESSIONAL Computer Science and Engineering, Indian Institute of Technology – Bombay, Mumbai, India

Project Research Associate

- Project: SanGeniX: A comprehensive Next Generation Sequence (NGS) data analysis solution.
- PI: Srinivas Aluru, Co-PI: Abhiram G. Ranade

IBM India Research Lab. (IRL), Bangalore, India

Research Intern

- Project: *Phase Identification in Smart Grids using Analytics*. From the time series data of meter measurements at the houses and at the transformer site, retrieve information about the electric phase each house is connected to, using LP based recovery algorithms.
- Was judged as one of the three best summer internship projects at IBM Research India.
- Mentors: T. S. Jayram, Vijay Arya

Texas Instruments (TI), Bangalore, India

Senior Software Design Engineer

- Worked with team to design and implement 'backward step' and 'backward run' feature in Instruction Set Simulators (ISS) for TI DSPs using lightweight check pointing
- Worked with team to design and implement enhancements to standalone (loader) client for ISS
- Design and implementation of software interfaces for integrating ISS to different IDEs TI Code Composer Studio, Vitio Virtual Platform Simulators, Mentor Graphics Seamless CVE

Software Design Engineer

- Implemented new features and improved performance of ISS for TMS320C54XX series of DSPs
- Implemented a multiprocessor ISS for TMS320C5421 DSP
- Designed a methodology to implement check pointing and restarting ISS for TMS320C55XX series of DSPs

PROFESSIONAL Conference Organizing Committee

• Foundations of Software Technology and Theoretical Computer Science (FSTTCS) 2011

Reviewer for Journals

• Theoretical Computer Science (TCS)

REFERENCES Dr. Abhiram G. Ranade

- Professor, Computer Science and Engineering
- Indian Institute of Technology Bombay, Powai, Mumbai, MH 400076, India
- Email: ranade@cse.iitb.ac.in; phone: +91 22 2572 7734

Dr. Srinivas Aluru

- Professor, School of Computational Science and Engineering
- College of Computing, Georgia Tech University, 801 Atlantic Drive, Atlanta, GA 30332
- Email: aluru@cc.gatech.edu

Dr. T. S. Jayram

- Manager, Algorithms and Computation
- IBM Research Almaden, 650 Harry Road, San Jose, CA 95120
- Email: jayram@almaden.ibm.com

July 2005 to June 2009

Autumn '05 Autumn '07, Spring '09 Autumn '06 Spring '07, Spring '08

January 2007 to June 2007

January 2013 till date

May 2011 to July 2011

July 2000 to June 2002

July 2002 to June 2005