Lecture 15
16 August 2018 11:37

memory virtualization.

design 0: restricted VA + 1-1 V2P mappings

design 1: base + bounds (limit) || multi-programming

1a. software-based relocation (static)

1b. hardware-based relocation (dynamic)

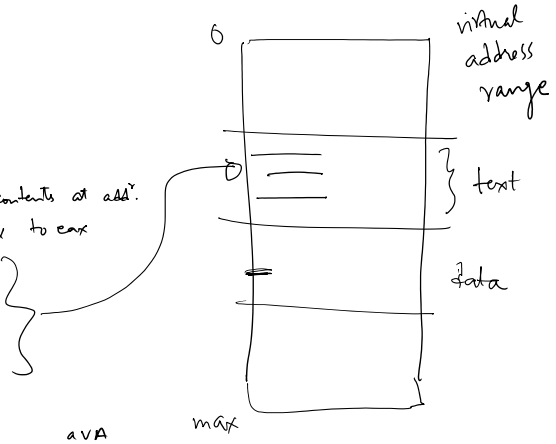
⇛ (PA = VA + base address) ← translation / mapping

example

```
x = 3000;
x = x+3;
```

```
mov (%ebx), eax
add  3, eax
mov  eax, (%ebx)
jmp  #EXIT
```

moving contents at addr. in ebx to eax



aVA

① fetch instr. from

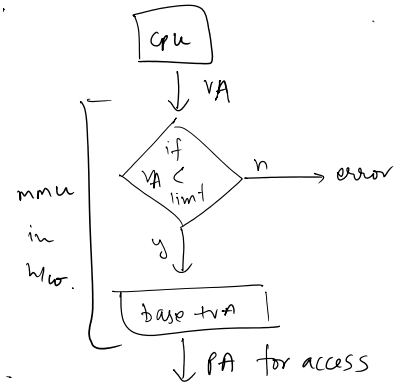
Execute (Load from %ebx)
addr in

Fetch inst.

Execute

Fetch instr.

Execute (Store to %ebx)
addr in

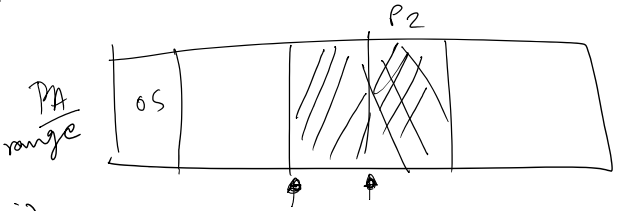


② H/w support

- CPU to have base & limit/bound registers
- h/w of CPU + MMU tightly coupled execution.
- ISA support of privileged instructions to update regs.
- ability to raise exceptions & regs. handlers.

③ OS implications.

(i) - free memory mgmt. — "what should be the base regs. value of a new process?"



(ii) ~ memory reclaimation

current assumptions

- ~~fixed sized processes~~ range — (1)
- VA range < PA range — (2)

(ii) ~ memory reclaimation

(iii) safe save & restore on context switch of processes.

memory context.
- base
- bound/limit

} part of PCB

(x) VA range < PA range — (2)

contiguous PA allocation (3)

(*) same sized processes. (4)

design 2: segmentation.