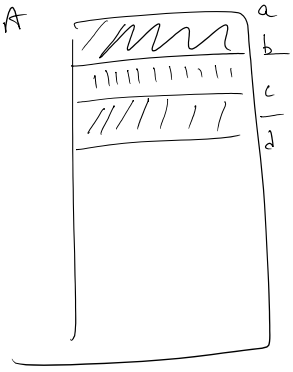
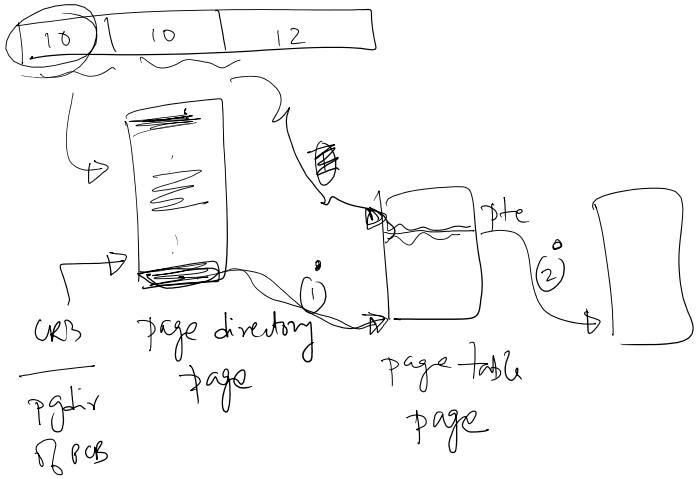


vma
① a — b
② b — c
③ c — d

- table design — # levels, page size.
- TLBs — address translation cache. || VPN → PPN
  - need for TLB flushes on context s/w.
  - Q. ~ valid partial flush on context s/w.
- $L = h \cdot T_a + ((1-h)\, W_a$ — memory access || translation latency.
  - T_a — access on hit
  - W_a — access latency of page walk

① Q. What happens when a VA has no page table mapping? (no valid)
- page fault occurs — interrupt — raised by mmu
- page fault handler
  - VA correctness check
  - "finds" page
  - map the page via page table

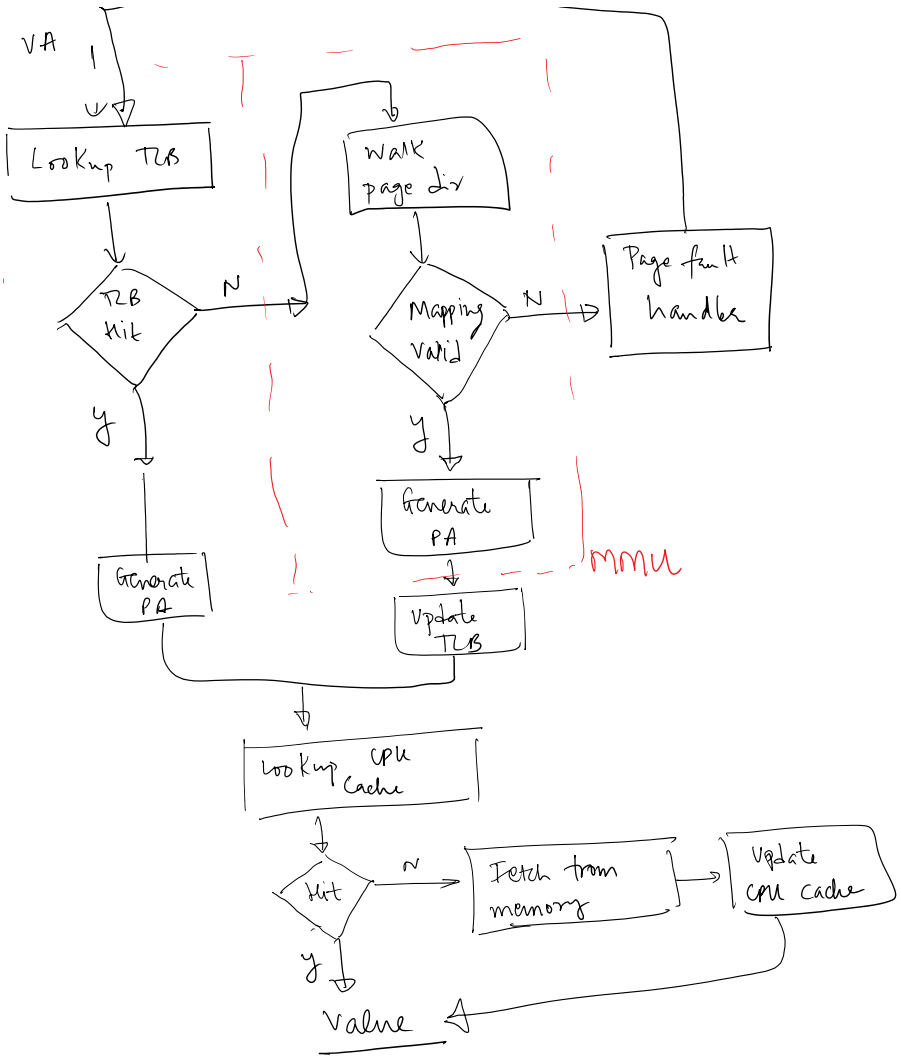
may involve evictions swapping etc.



- "reissue" faulting instruction.

② 

(2)



(3) invalid mappings (generate page fault)

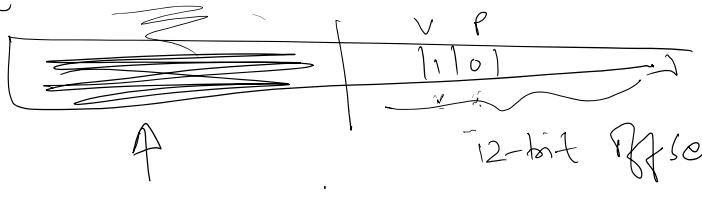
- no mapping
  - no mapping ever created
  - mapping currently not available.
- ~~no~~ permission violation.

PDE } flags — residual LSB 8 bits of a page table entry.

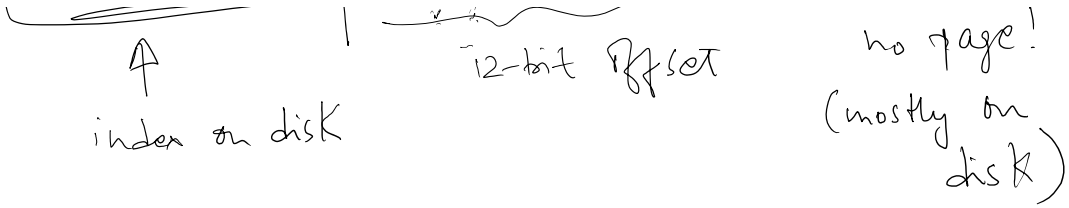
— VALID — 0/1

PRESENT — 0/1

PTE



← mapping valid no page!


index on disk
12-bit offset
no page!
(mostly on disk)