

von-neumann model:

fetch (from address stored in PC)
location

decode

execute — (may update PC)

repeat

- Lab2 will be out this week.

OS requirements

- useful abstractions
- efficient resource usage
- ~~robustness~~ / failure handling
- isolation / "contained" interference
restricted

Challenges

- ~ monopolizing resources
- ~ unintended state / data memory sharing

e.g.: interval timer register ~ reg. available in some ISAs

that counts down &

on zero stops the

current app'n.

on CPU to

possibly do

something else

(execute different application)



who/which entity
 updates the interval timer
 registers?

main invariant / condition for design

of all OSes.

⇒ the OS is the sole owner / arbitrator
of all resources (hardware resources)

CPU,
disk, network,
memory . . .

 two main design principles / building blocks of an OS.

(i) limited direct execution ~ LDE (on the CPU) } privilege levels of execution.

(ii) interrupt-driven execution.

(i) LDE ~ ISA supported feature

~ the CPU executes with a privilege level

~ the PL can be self-updated

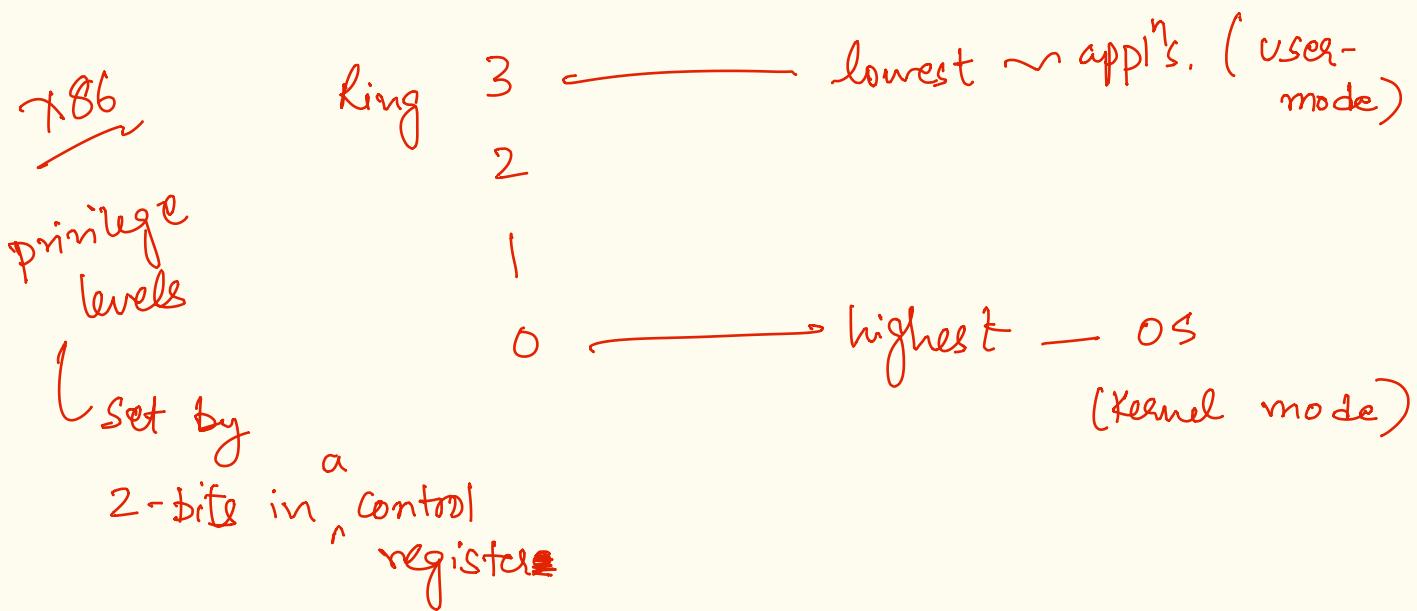
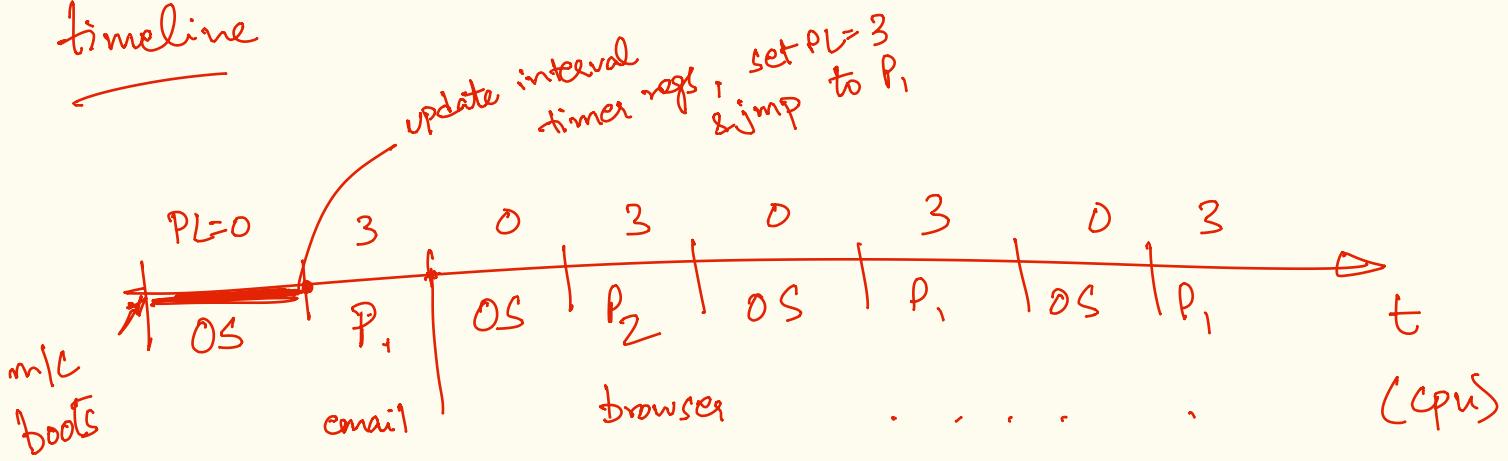
~ every instruction of the ISA has a minimum

privilege level specified for correct execution semantics.

~ critical / sensitive
instructions

alter system usage
behaviour

Timeline



(ii) interrupt-driven execution / interrupts

what is an interrupt?

- ① interrupting / pausing / stop the current sequence of instructions
 - ③ after ^{current} instruction executed, the PC changed to jump to some other location.
 - ② * Save state of current execution
 - PC
 - cpu registers.
 - ③ go to $PL=0$ & jump to a locⁿ in the OS program
- $\xrightarrow{\text{mov } 23, \#b}$
 $\xrightarrow{\text{add } \#b, \#a}$
- ← interrupt

why interrupt?

- ↳ ~~most~~ everything in the world are non-deterministic!
- ↳ all IO is non-deterministic (in time)
 - ↳ KBD / mouse
 - ↳ disk read
 - ↳ arrival of new packets

types of interrupt

- ↳ hardware → IO
- ↳ software
 - implicit
 - explicit
 - ↳ exceptions
 - ↳ div by zero
 - null ptr.