

CS 744

Lecture 11

Lab Quiz 1

the address space

today: 2nd Sept.

5.30 pm

SL1 & SL2

VA $\rightarrow$ address $\rightarrow$ PA
translation

①

segmentation & paging.

(multi-level)

base
segment register
segment limit.

pgd — page directory
ptr.

xv6: riscv — ^{S39}long mode

on an 64-bit address bus

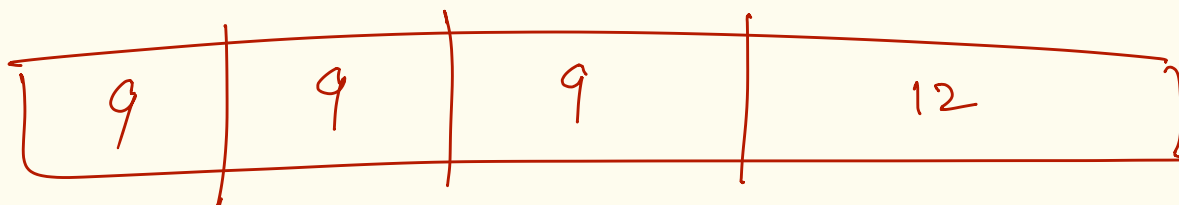
only 39-bits of LSB are interpreted
as an address.

uses only 38-bits of LSB for
its address space — $\text{MAX VA} = 2^{38} - 1$

256 GB

Pte size: 8 bytes | page size
= 4096 bytes.

VA:



H.W
①

~ x86: 48-bit mode

⇒ pte: 8 bytes

⇒ page size: 4096 bytes.

Solⁿ: ~ 4-level page table!

② what if size of pte = 16 bytes?

③

8	4	8	12
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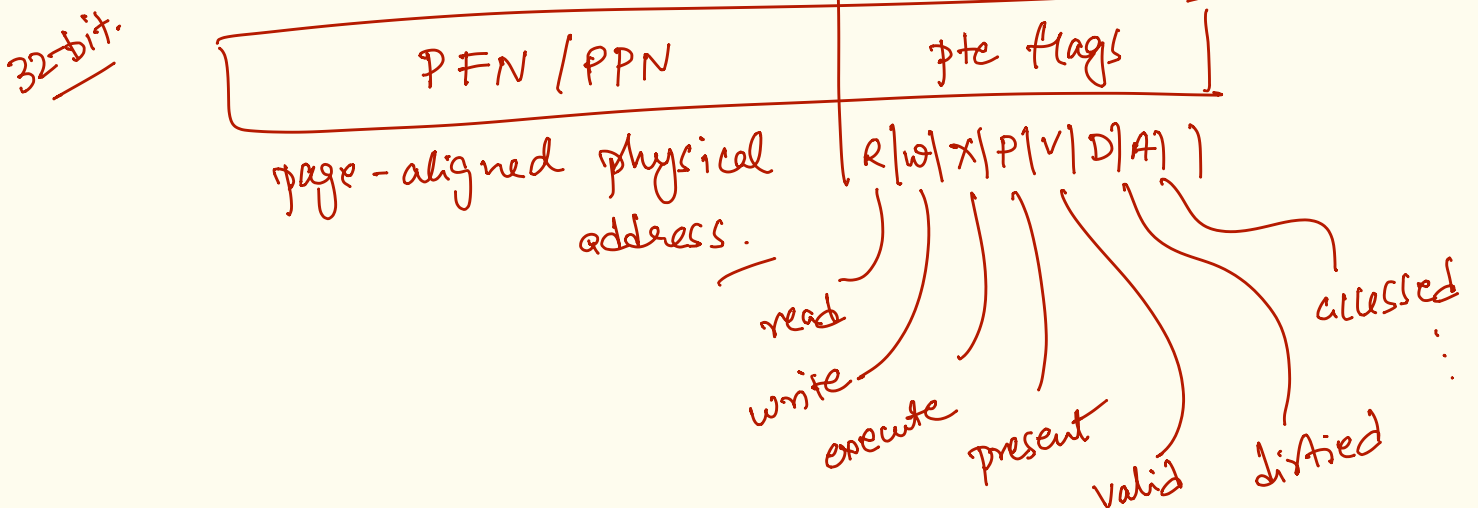
 (VS)

4	8	8	12
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 ✓

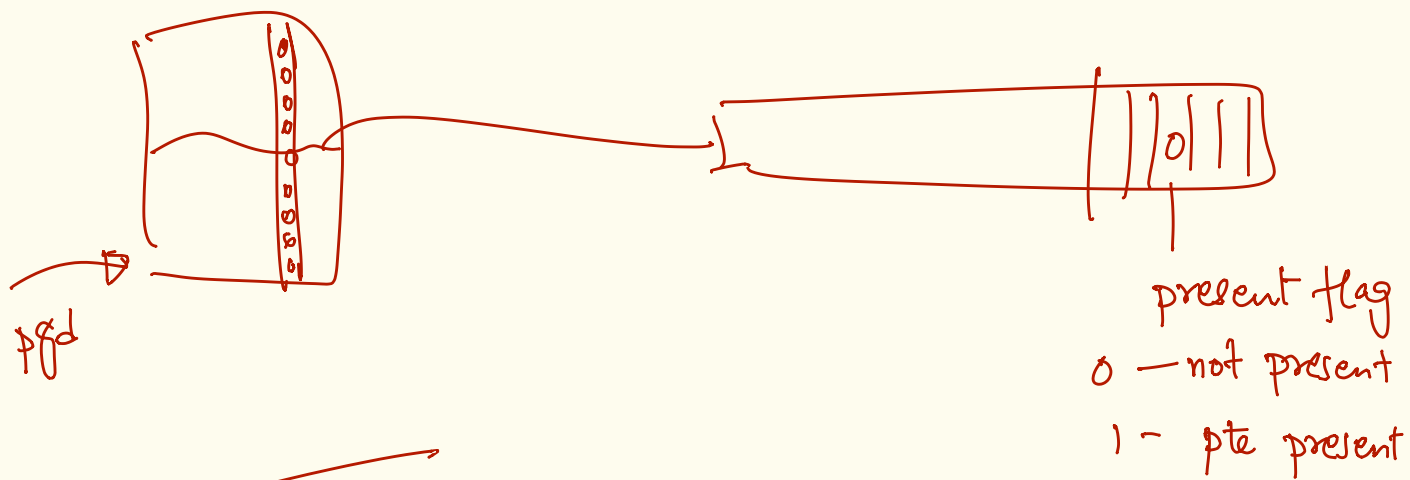
④ page table configs ⇒ diff. configs have different tradeoffs.
(memory req. & performance of the page table.)

② pte flags.



Q which entity/entities access & modify the pte flags?

↳ OS & the MMU



COW

COW

— sets pte flags : $R=1$
 $W=0$

on write

page fault

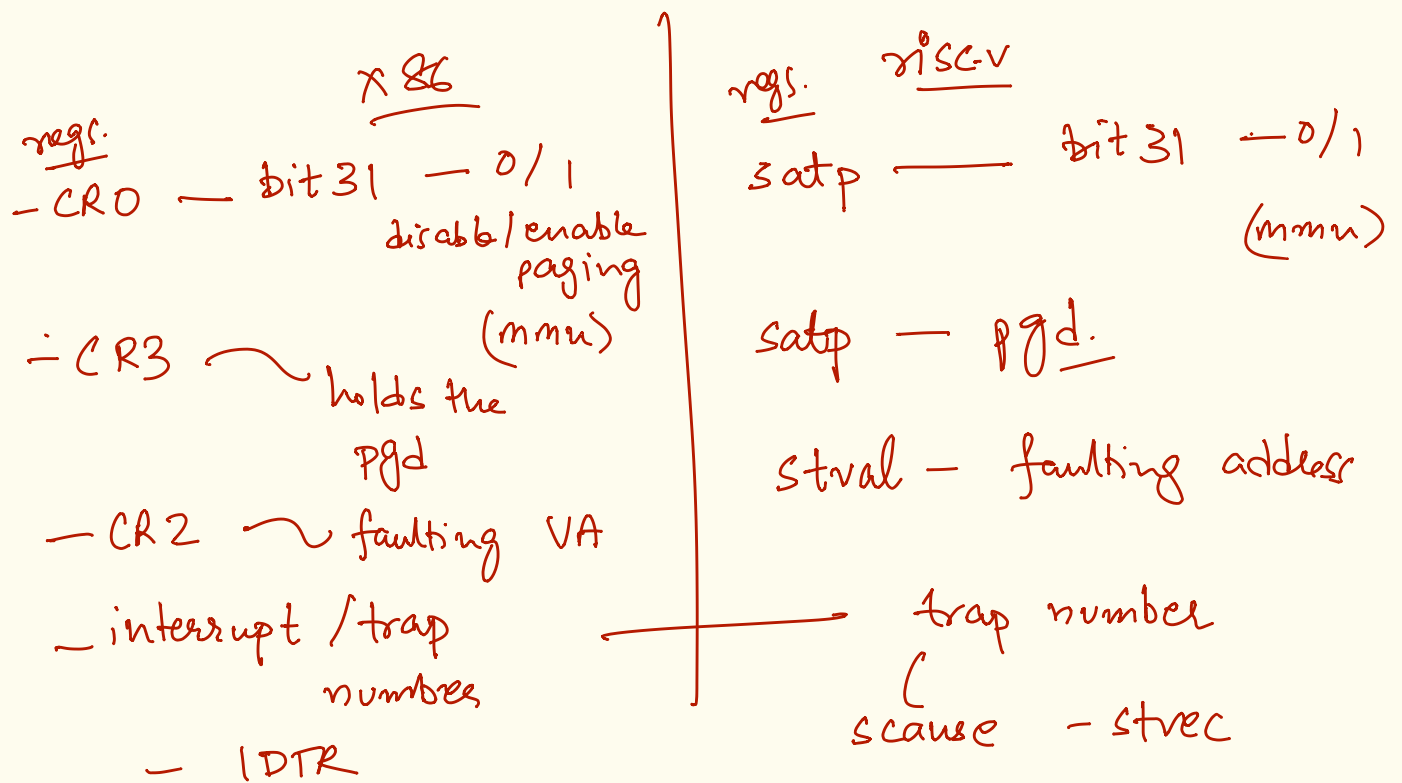
fault handler

allocate new page
copy contents

update page tables $R=1$
w/ pte & pte flags $W=1$

③ ISA support for the address space abstraction

- real mode, virtual mode
 └ segmentation
 └ paging.

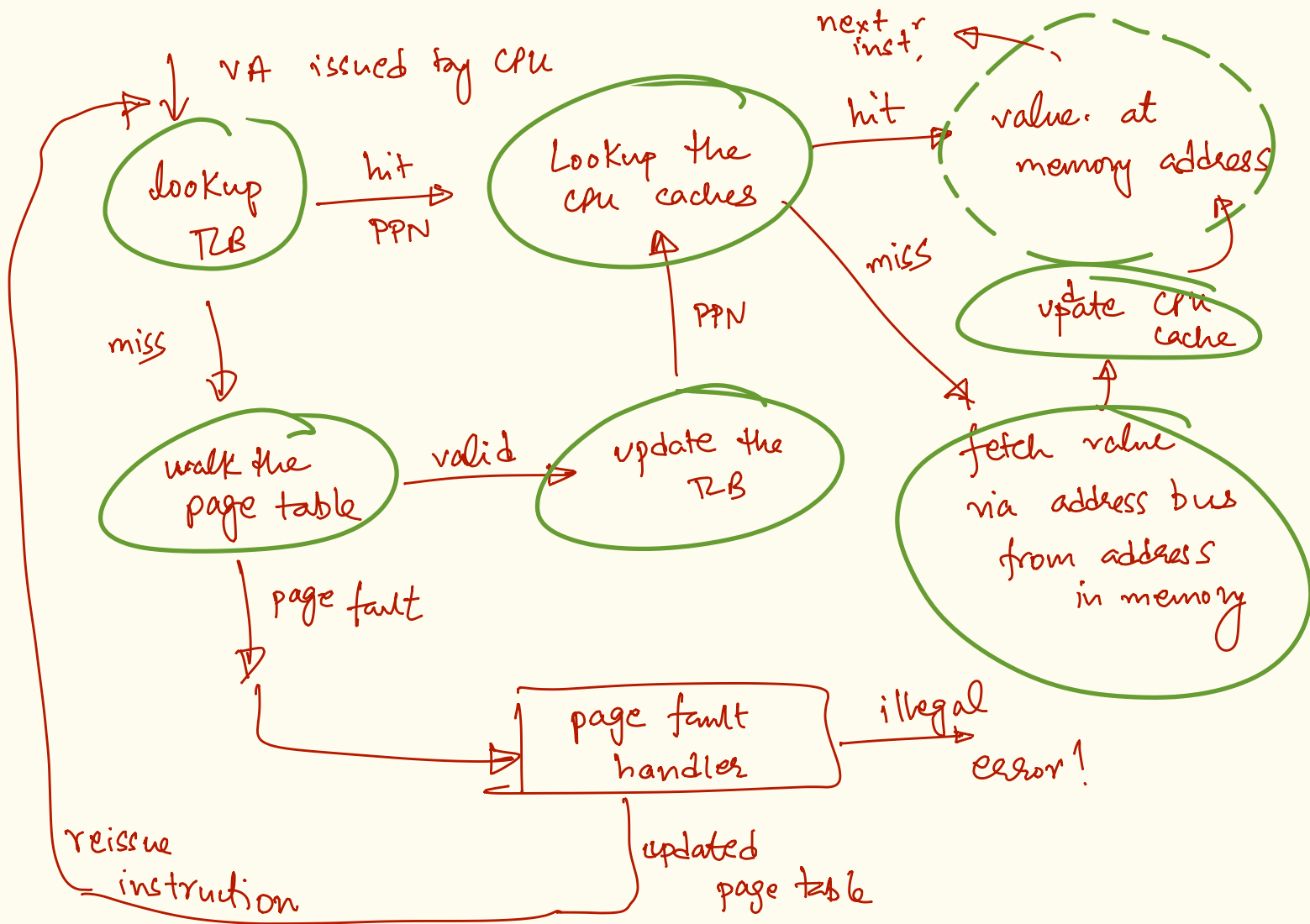


④ TLB — translation lookaside buffer
 └ CPU cache which stores

~~VA — PA~~
 VFN / VPN — PPN / PFN

⑤ CPU L1/L2/LLC — caches.

~~VA~~ → value / data
 PA → value / data



type of faults.

(1) cow $\longrightarrow$ $\frac{\text{VA's}}{\text{VPNs}}$ sharing single PPN

pte: $R=1, W=0, P=1, V=1$

(2) exceptions $\longrightarrow$ no $V \rightarrow P$ mapping
 $P=0, V=0,$

(3) lazy allocation $\longrightarrow$ VA is valid but $V \rightarrow P$ missing!

(4) swapping $\longrightarrow$ VA is valid but contents of mapped PA are currently on disk!

$P=0, v=0$

but VA is valid

$P=0, v=1$

— mapped page is
on disk.