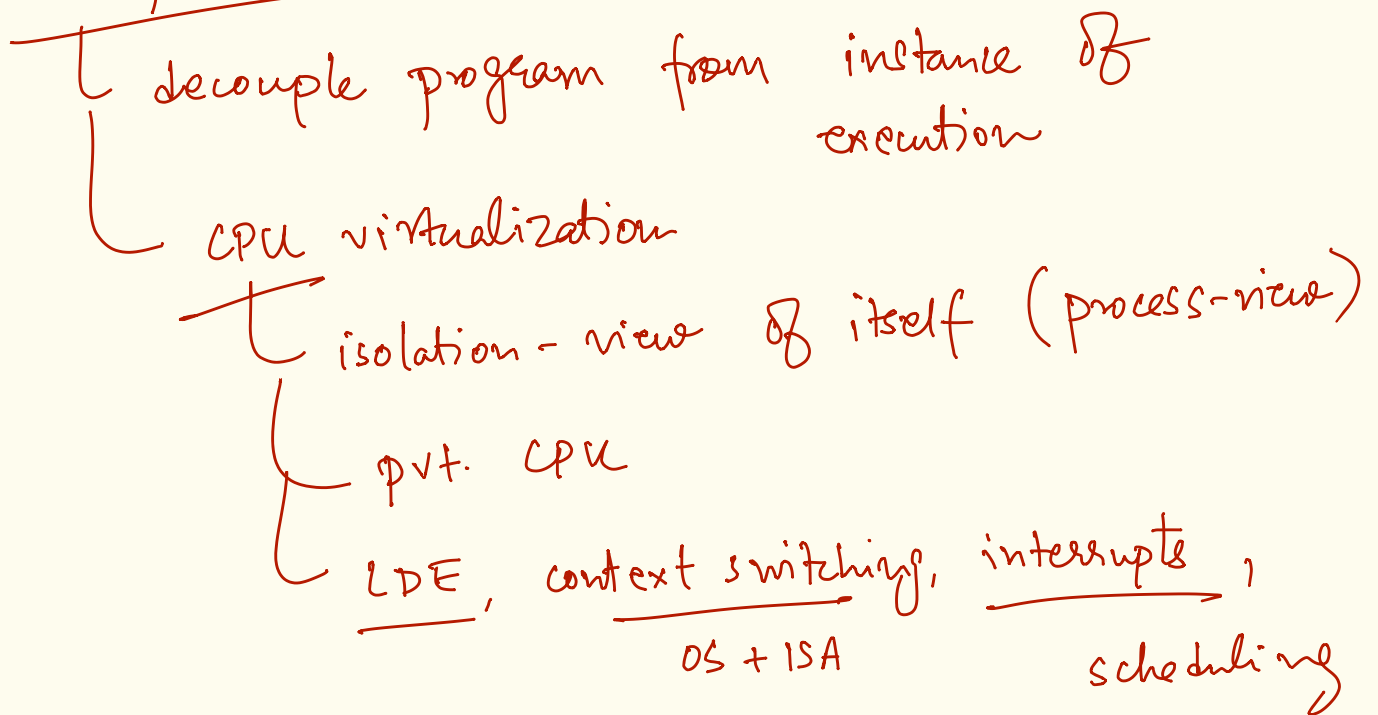
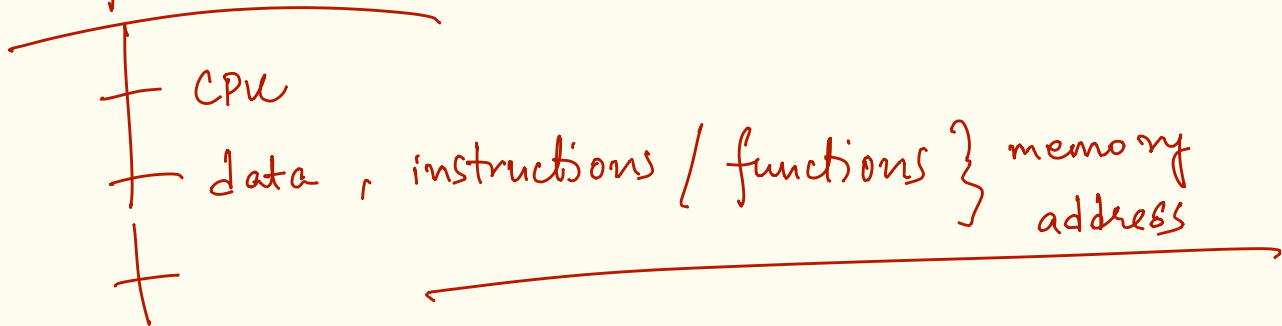


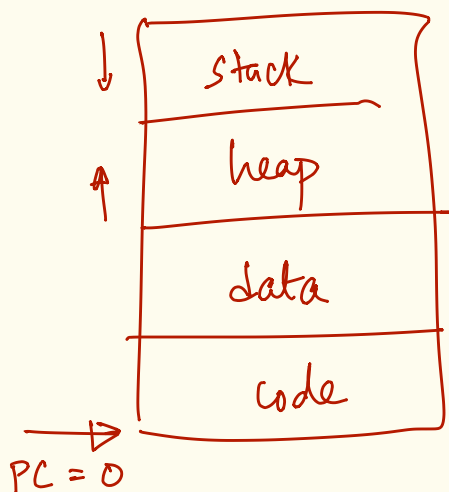
## # the process abstraction



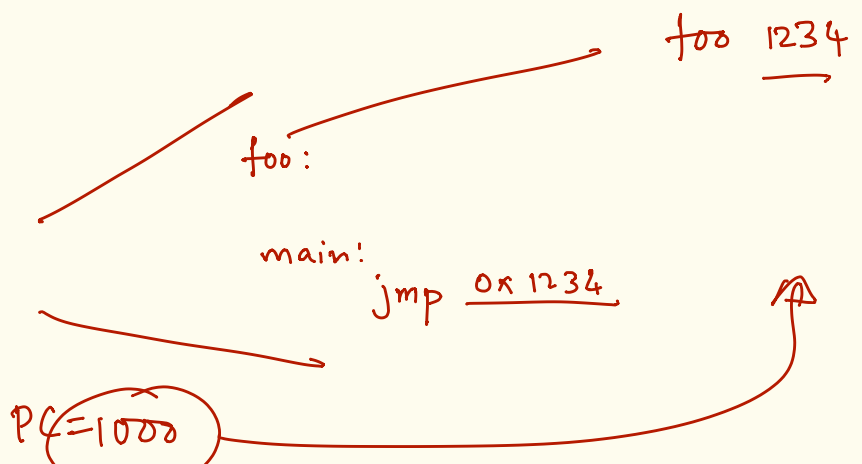
## ⑧ process-view of system



## process-layout in memory



— this arrangement has to be consistent across all processes.



# the address space abstraction for every process.

└ has a 0-starting address range

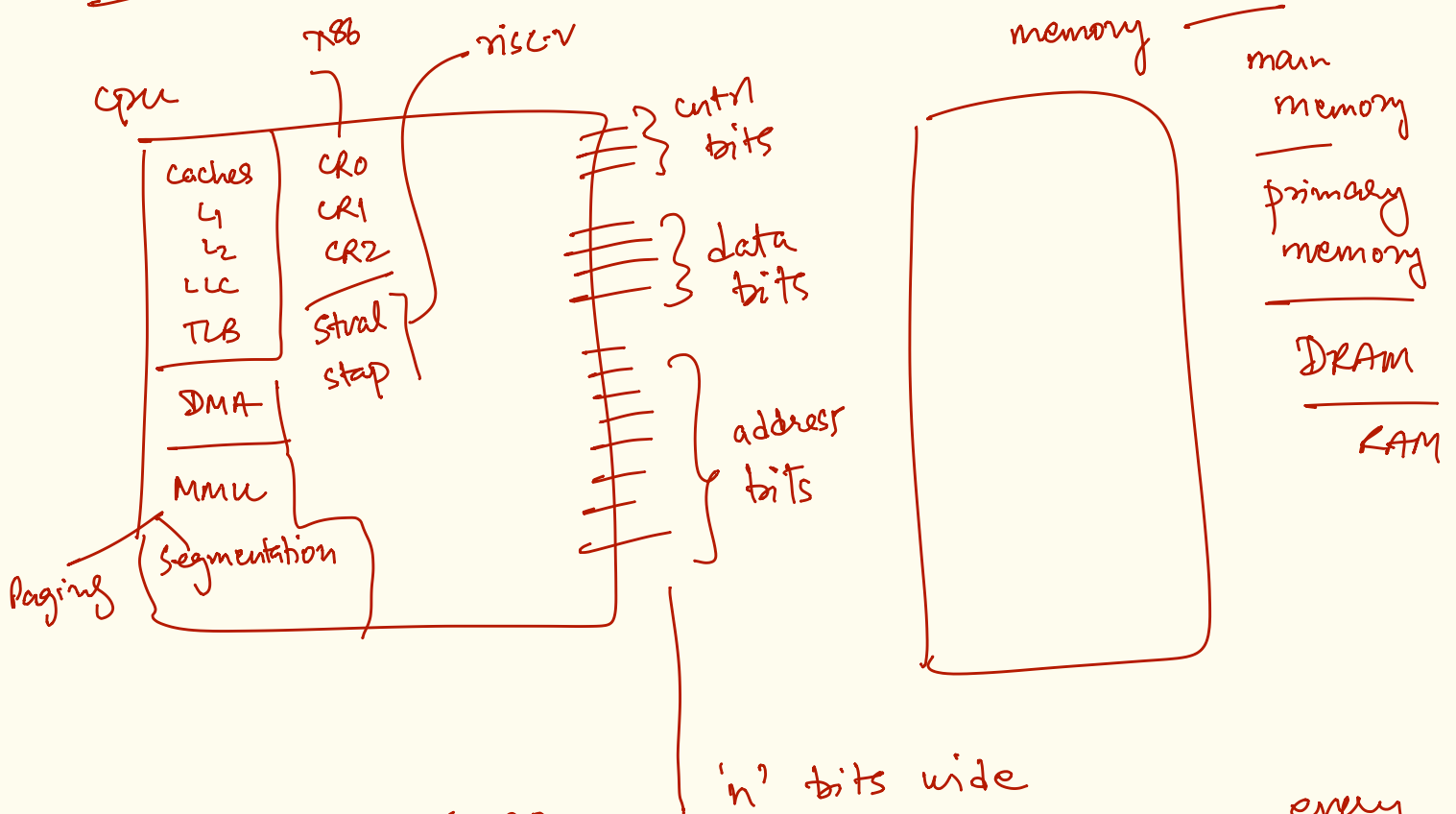
└ 'full' addressable range

+ task of the OS

└ implement the address space abstraction

w/ transparency, efficiency, isolation

# ISA - view of memory!



range  
of addr. :

$$0 \text{ --- } 2^n - 1$$

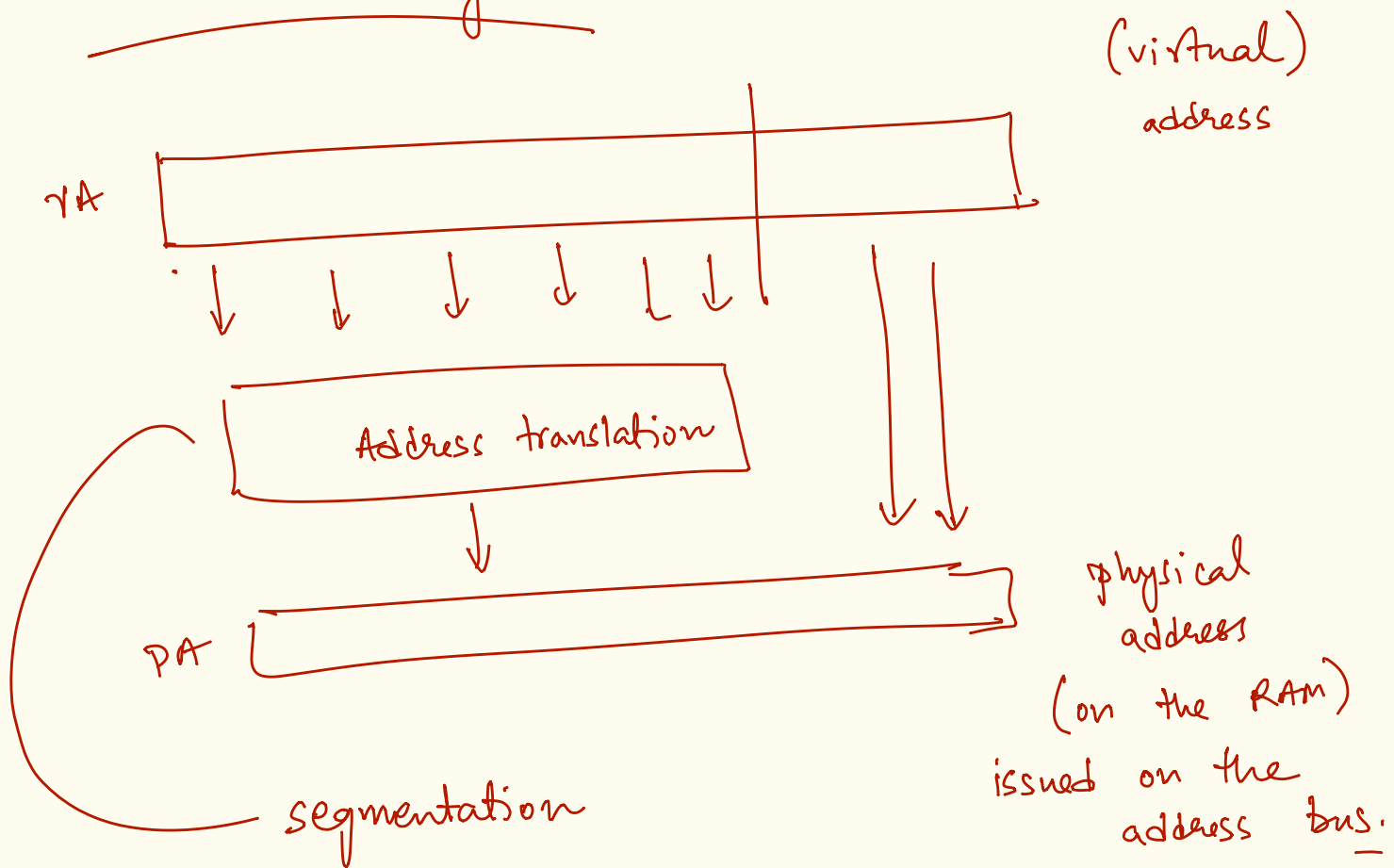
addresses.

if  $n=32$

$$0 - 2^{32} - 1 \Rightarrow 4GB$$

every  
address  
addresses  
one byte.

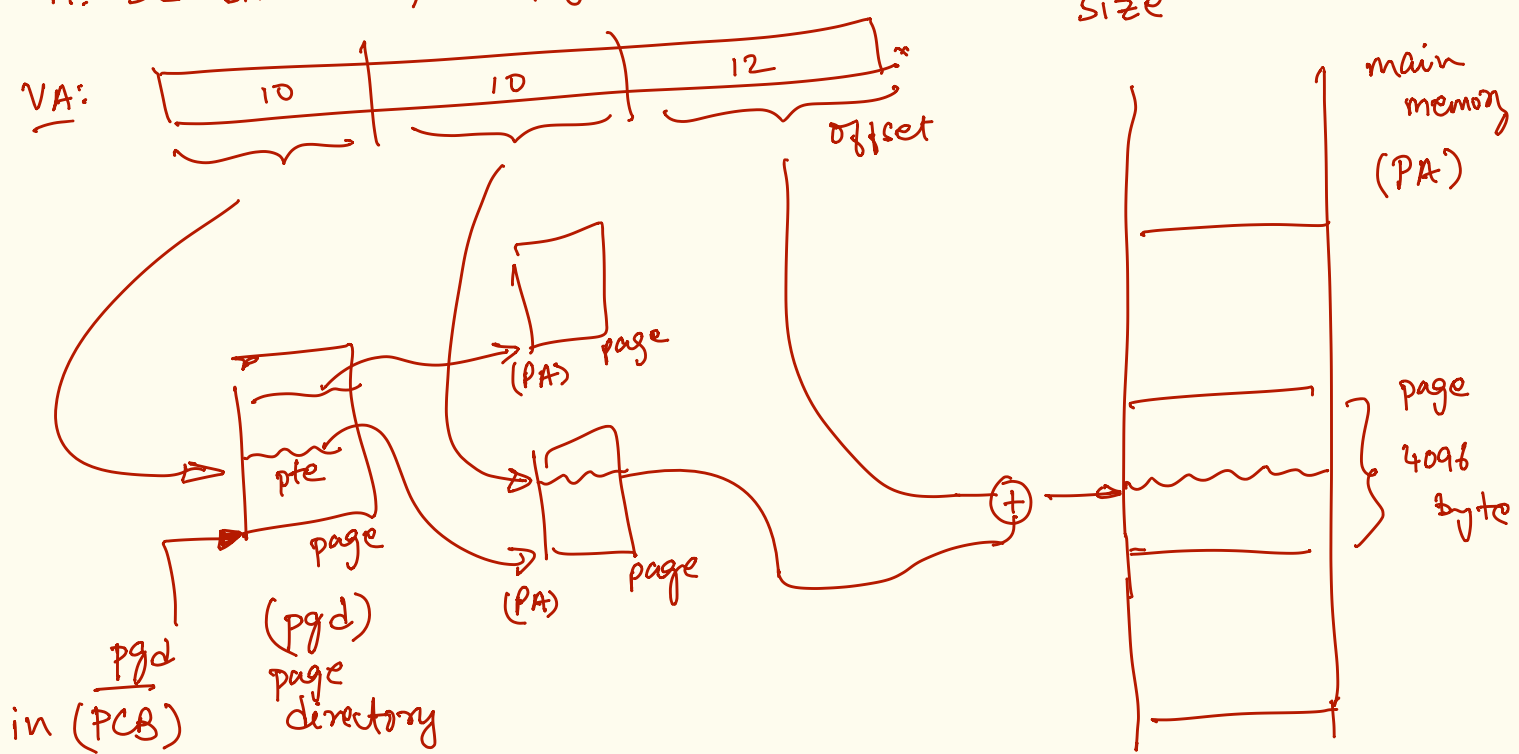
# the # virtual memory mechanism



## paging.

④ dividing all memory mgmt in fixed-size granularity — page.

n: 32-bit CPU, page size = 4096 bytes, pte = 4 bytes size (page table entry)



$2^{32} \sim$  addresses

$$\# \text{ pages} = \frac{2^{32}}{2^{12}} = 2^{20} \checkmark$$

pte size = 4 bytes

$$\frac{\# \text{ ptes}}{\text{page}} = \frac{2^{12}}{2^2} = 2^{10}$$

page = 4096 bytes

1  
12 bits.