

Lecture 5

CS 695

cpu virtualization for VMs.
with

recap: trap-and-emulate
binary translation / trap-and-emulate.

AI

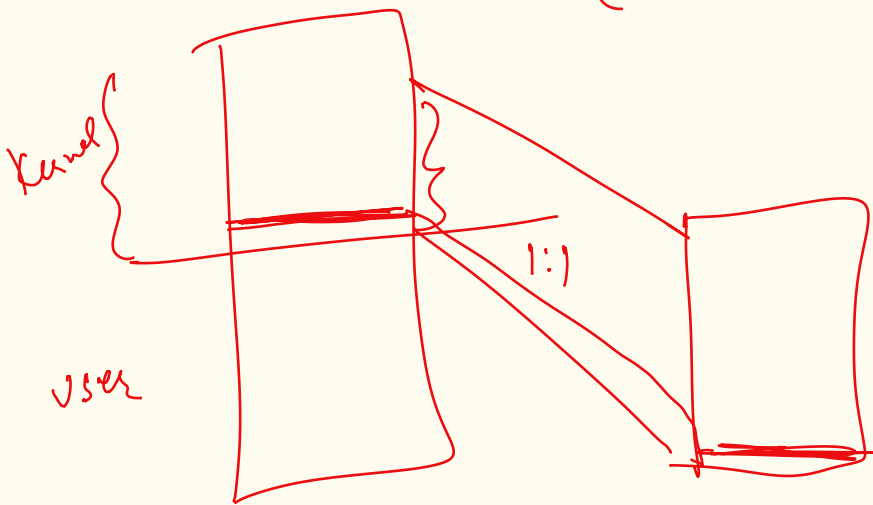
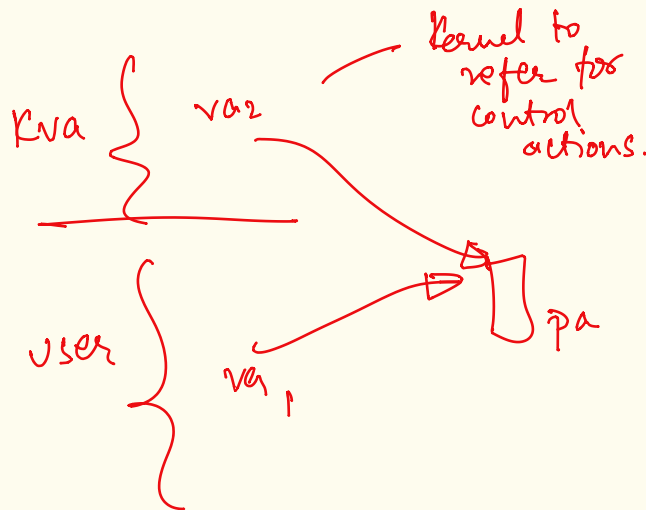
user space

P
get pa(va);
write to pa(p, val);

Kernel.

x = val; (x)

↑
va
inverse lookup
va (va)
user in process address space
va2 (kva)



~~(kva - OFFSET) → pa~~

kva : kva - OFFSET
VA PA

virt 2 phys
kva → pa
→ kva
pa ← kva

Design 3: paravirtualized approach for cpu virt.

⊛ Guest OS knows about the vmm vm abstraction.

⇒ not issue problem instructions!

⇒ enabled via a mechanism: hypercalls.

hypercall: similar to the system call interface

⇒ interface between Guest OS the hypervisor
(abstraction) VM

⇒ explicit invocation.

int 0x80 — x86 syscall

int 0x82 — hypercall [xen]

↑
provider
of abs.

idea: on any critical work

~ anything that needs
hypervisor intervention

explicitly make a hypercall.

Guest va → pa ?

0x2000 → 0x4fffaabab
?

e.g.: mmu-update (va, pa, pte details)

representative
hypercall.

↓
pa_x

① ~~try~~ trying to update page table.

② setup the IDT.

G&P 1974

↑
needs
Guest OS changes.

— PV'ed OS

efficiency — ↑
control — ✓
equivalence — ??

Design 4 : hardware-assisted virtualization ~~of~~ support for the CPU.

② h/w architecture redesign/upgrade to support system-level virtualization.

key idea: programmatic control of traps || exits config.

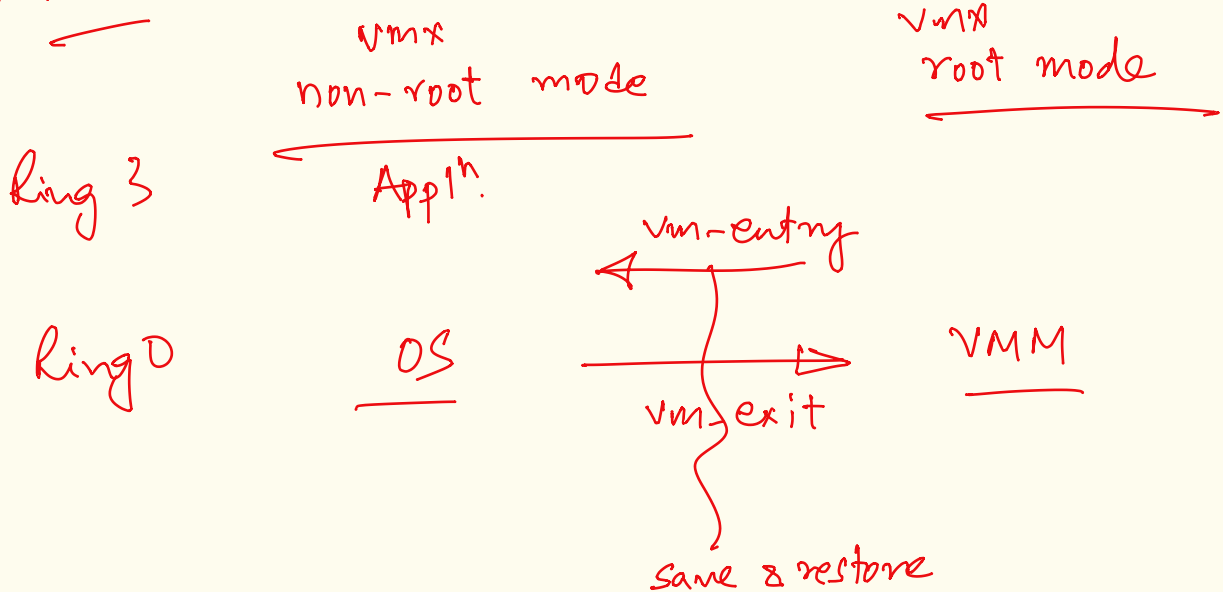
— x86 ISA

(i) vmx modes of operation

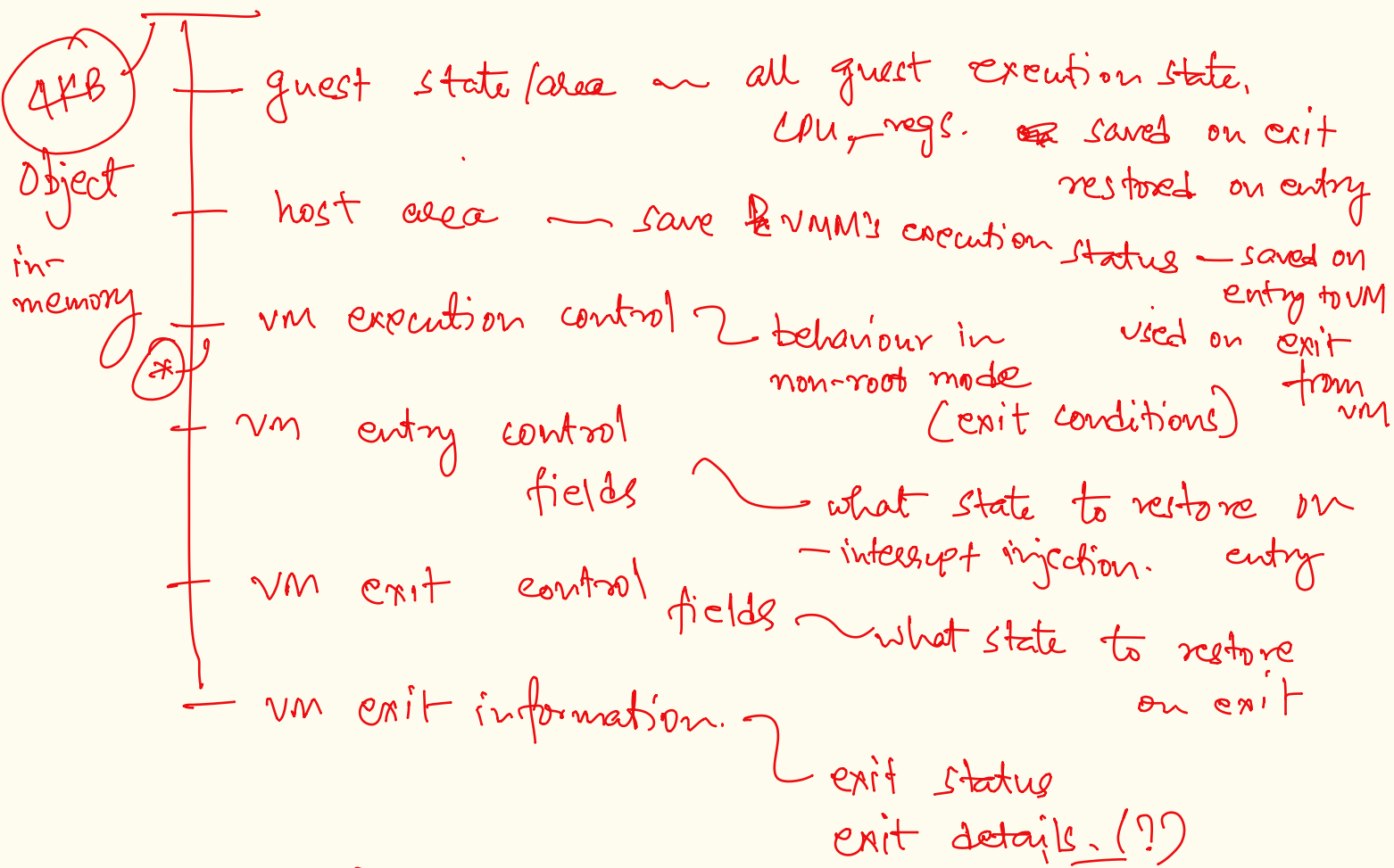
(ii) vmx instructions

(iii) vmx state (context & config.)

→
— vmx modes.
(i)

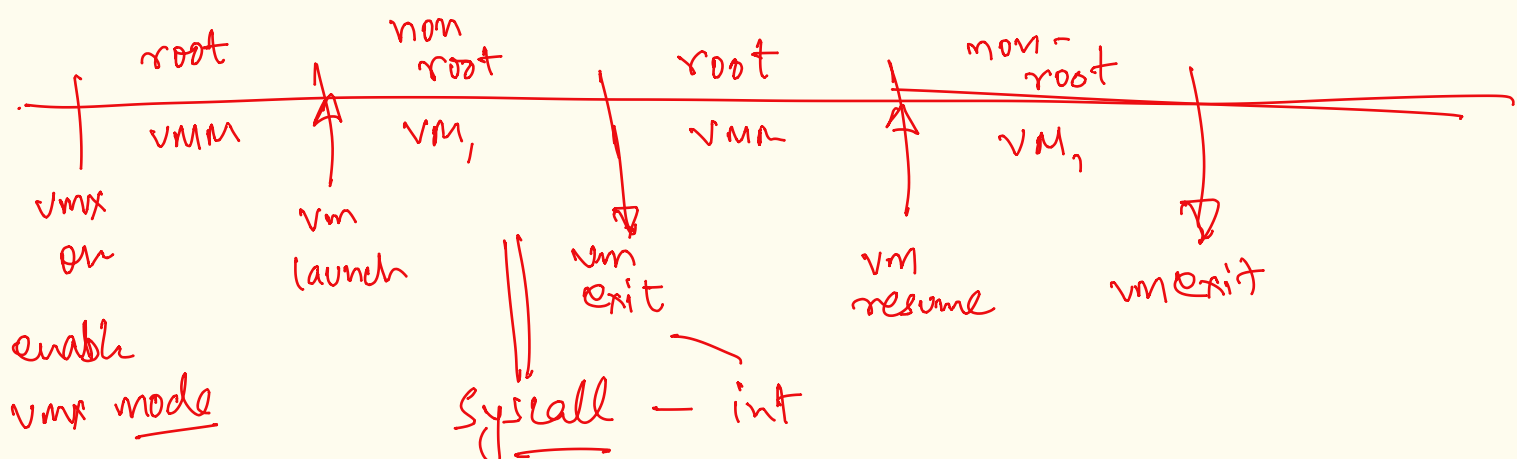


VMCS : virtual machine control structure



* the new privileged instⁿ

vmread vmwrite ~~vmclear~~, vmhlt ptr
 vmx on vmx off vm launch { vm resume vmexit } // ISA
 - per-cpu vmcs ptr. (regs).



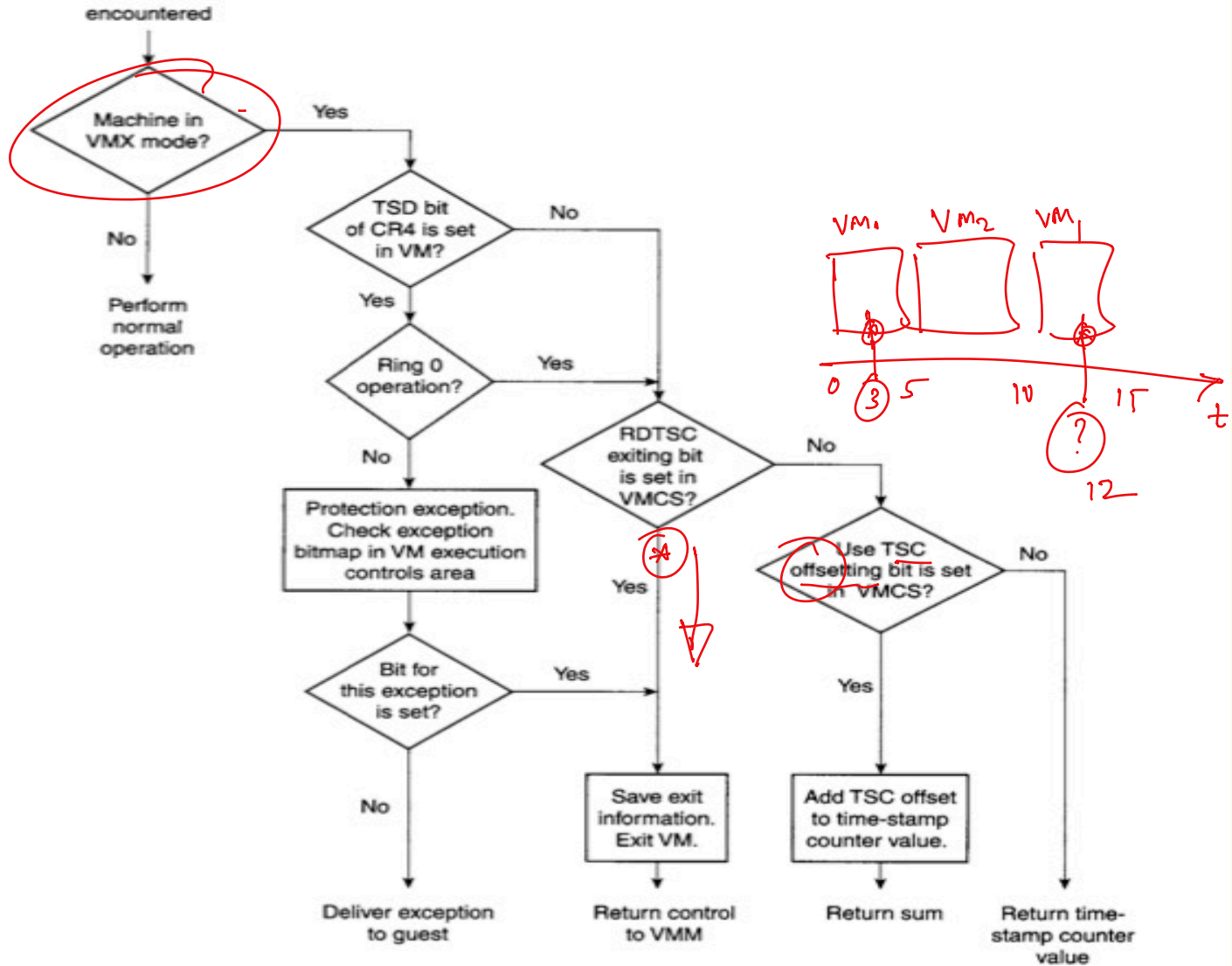


Figure 8.27 Actions Taken by Hardware When a Read Time-Stamp Counter (rdtsc) Instruction Is Encountered.