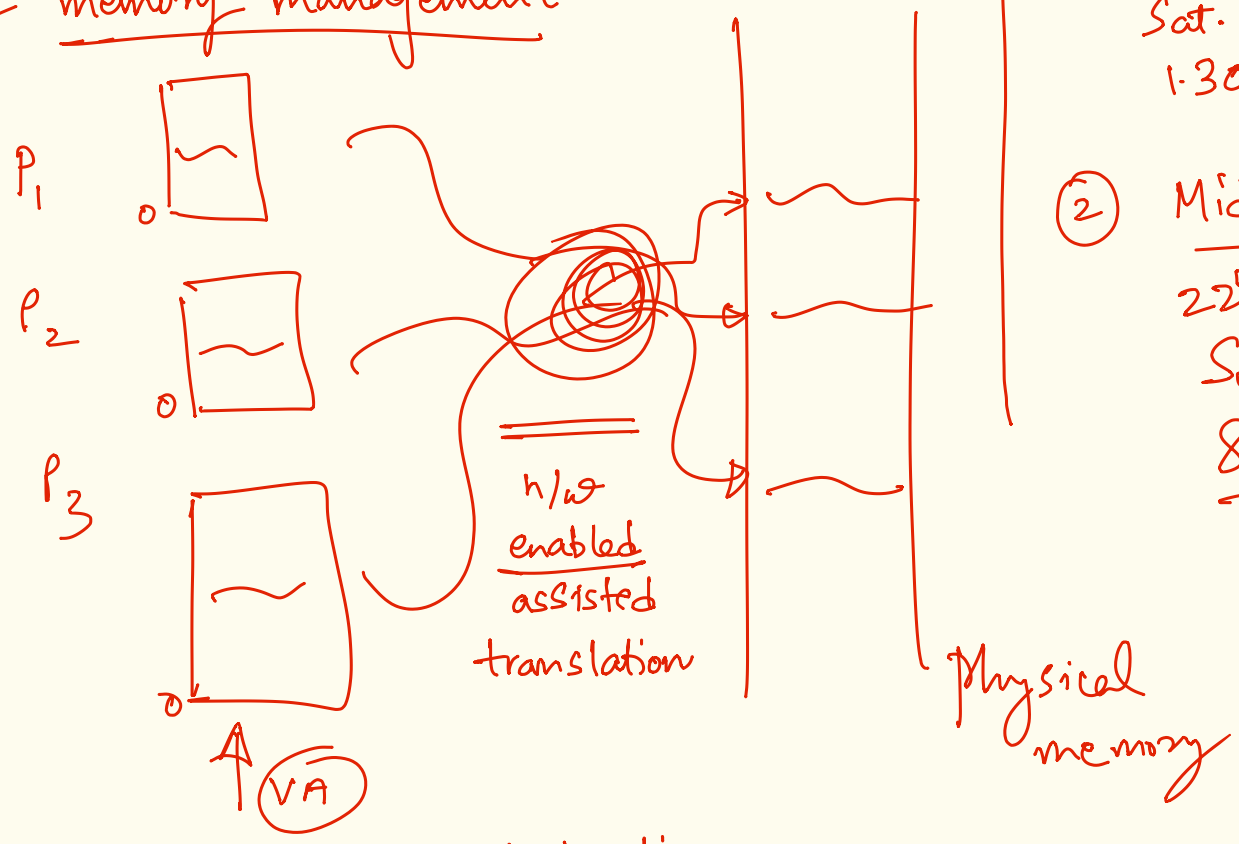
CS 219 Lecture 15

① Labquiz 2
21st Feb.
Sat.
1.30 pm

② Midsem
22nd Feb.
Sun.
8 am

memory management



the address space abstraction

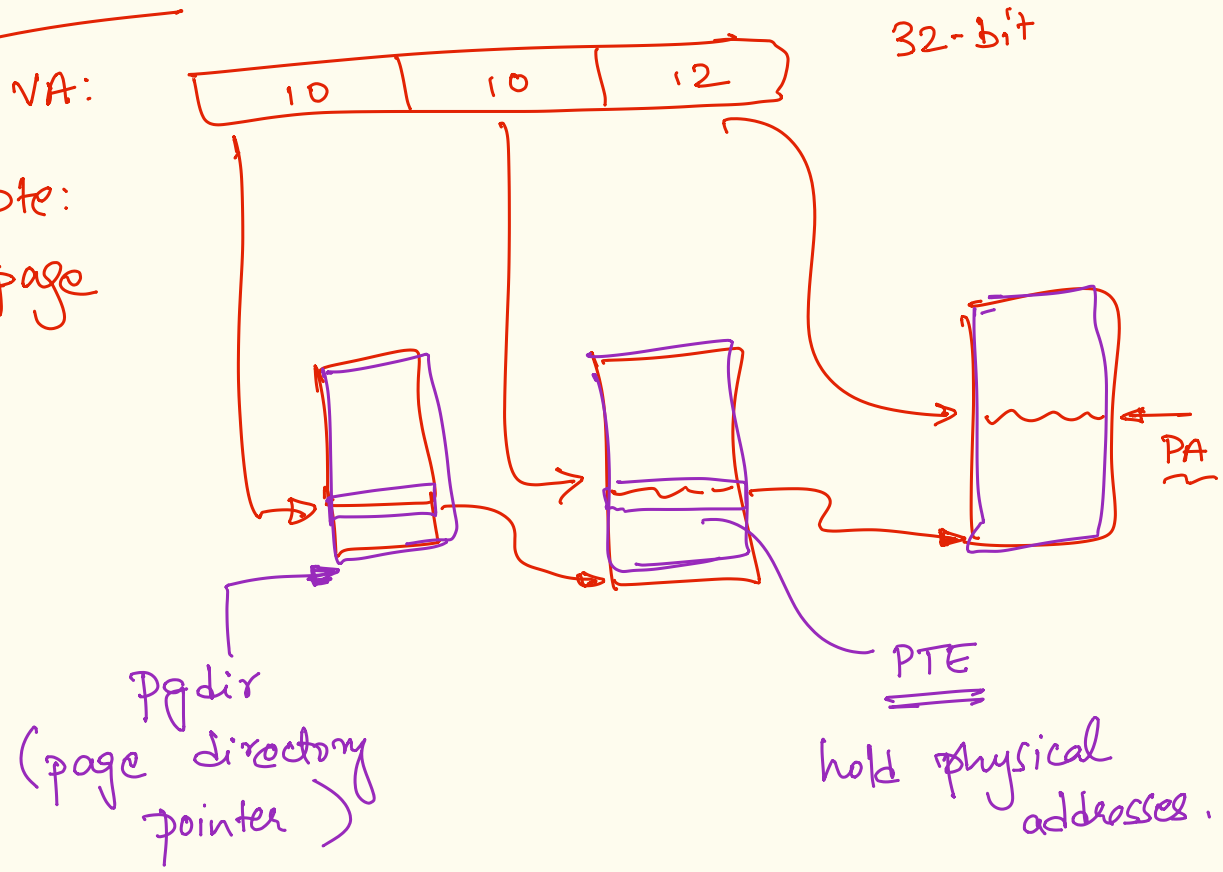
paging

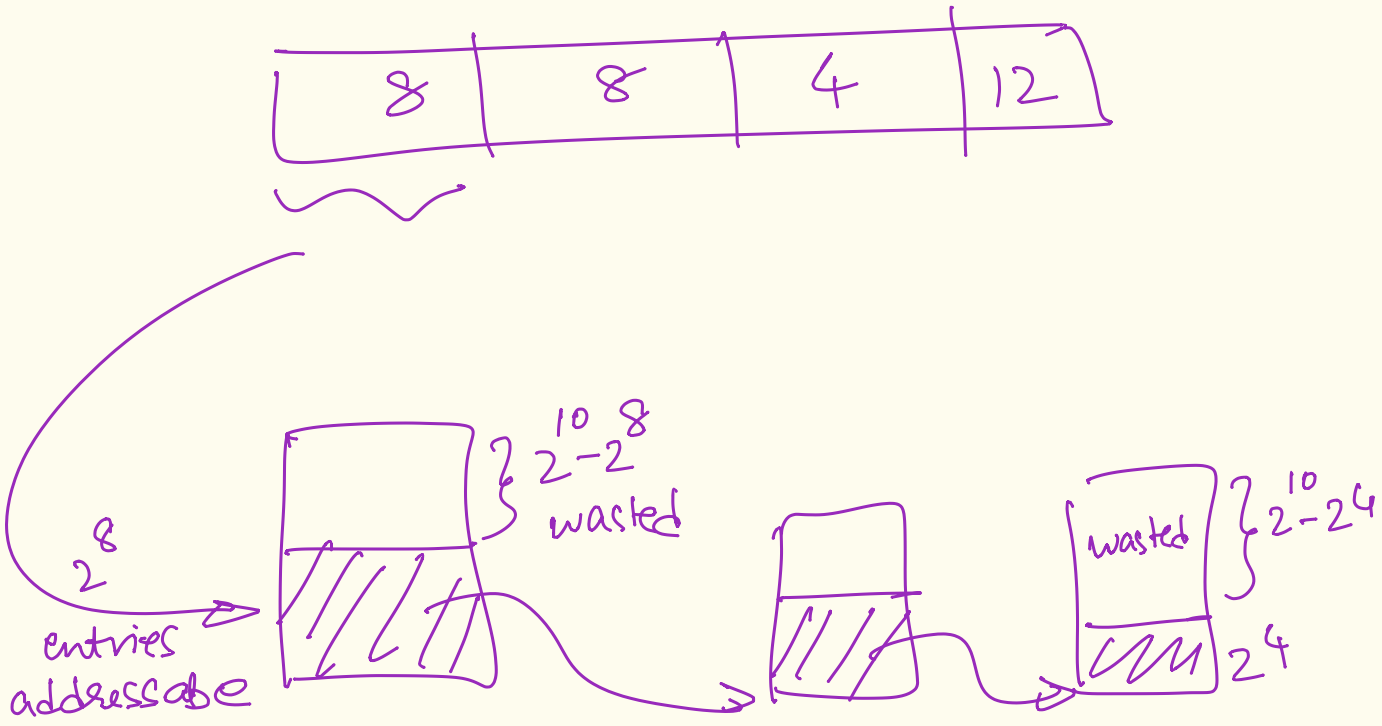
- every address issued by the CPU is treated as a virtual address.
- paging enabled/mode of the CPU
  - real mode vs. protected paging mode
    - all addresses on CPU are physical addresses
    - all addresses are virtual addresses & needs translation.

CR0 ~ Control registers — bit to enable/disable real mode

x86: segmentation and/or paging

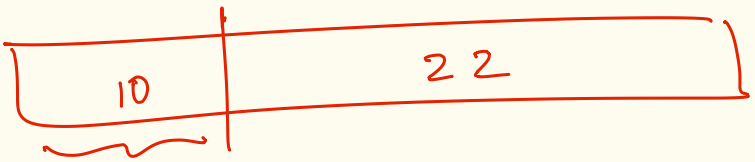
page table ~ is the translation metadata.

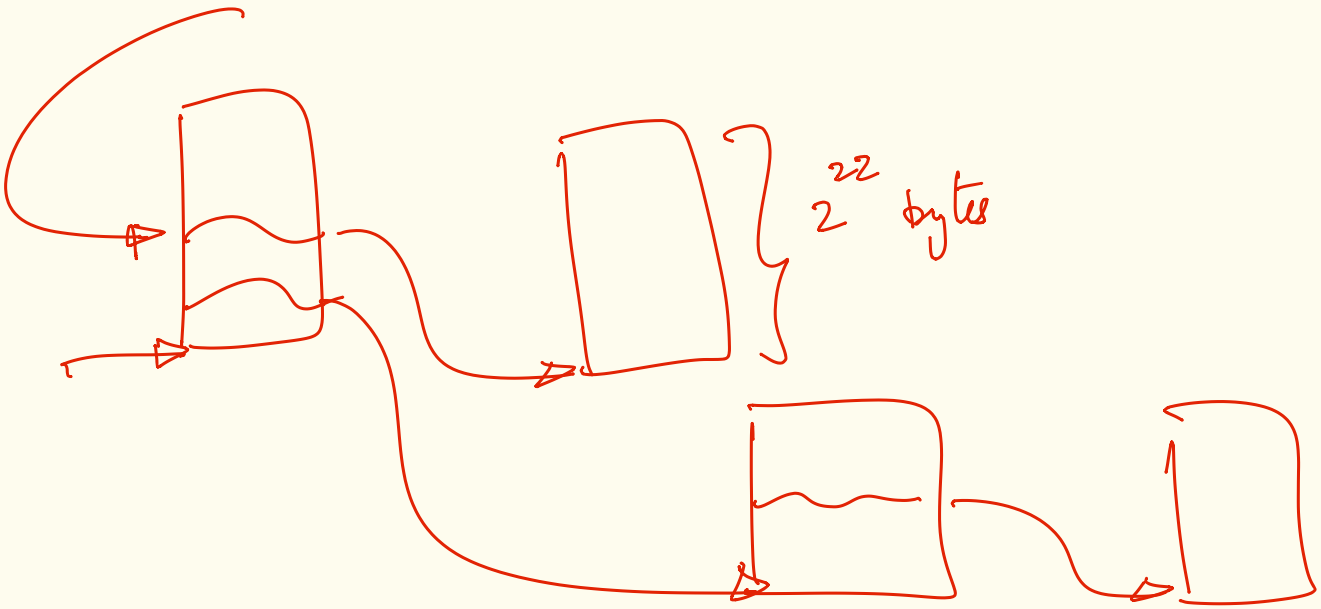




VA:

VA:



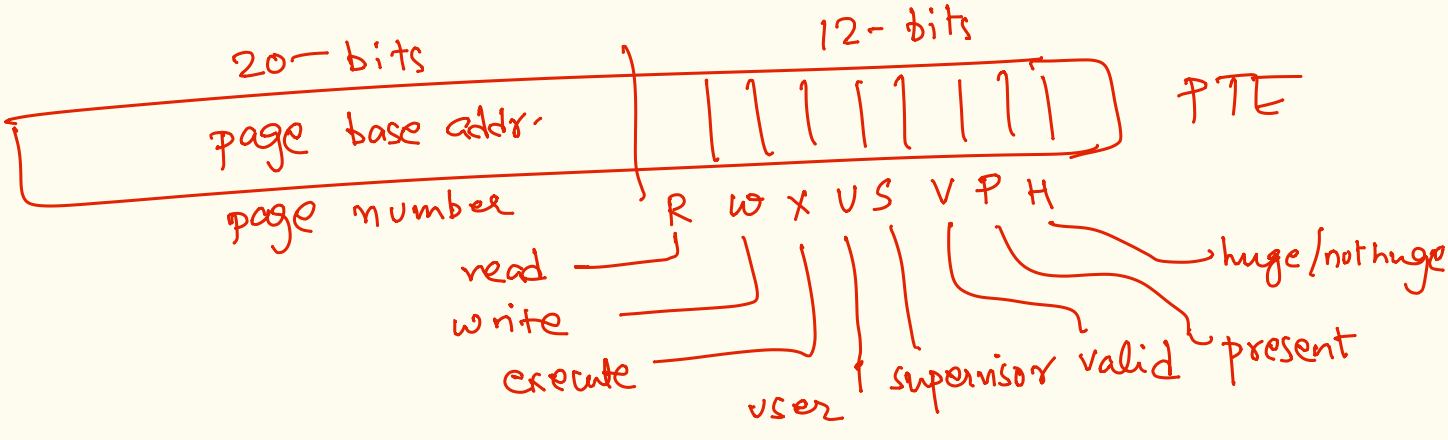


pte flags

LSB bits of a PTE

32-bit PTEs, 20 bits of MSB point to start of page

12 LSB bits are the flags.



MMU : the ISA h/w translator

- given a VA
  - uses loc^n of pgdir for pgtable walk

x86	risc v
CR3	satp

- use offset of VA + pte flags

to interpret PTE & proceed to next level of page table.

or not & raise an exception / interrupt

⇒ page fault!

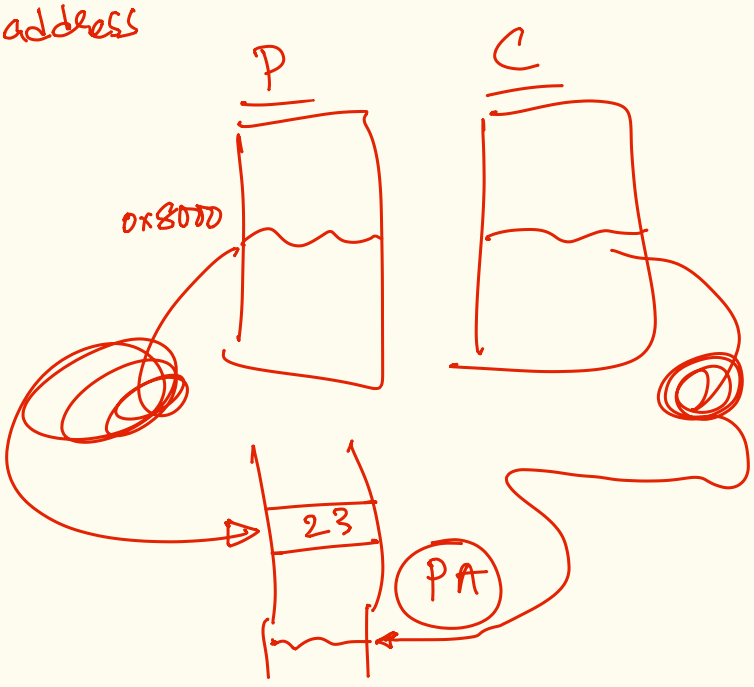
(#)

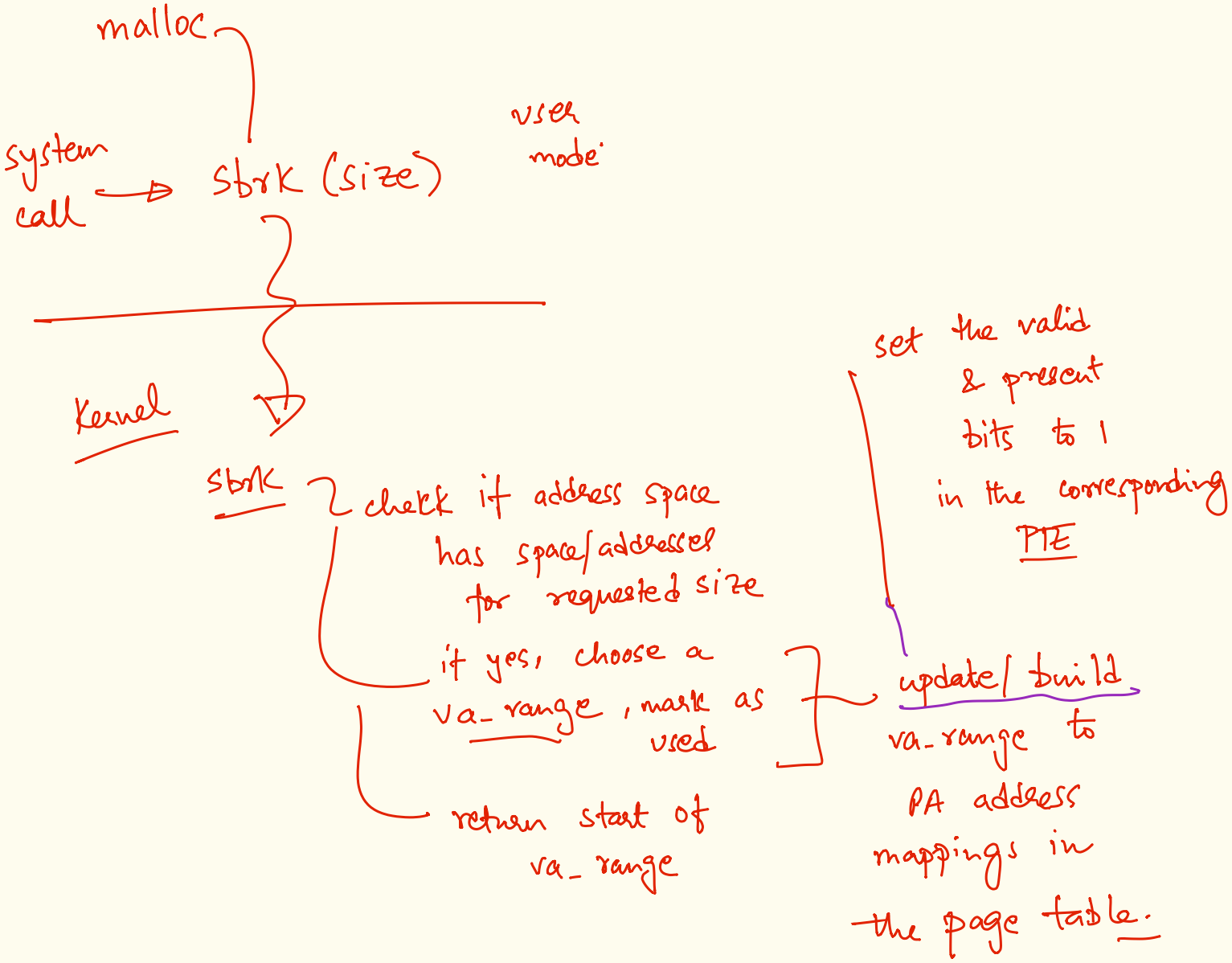
```
int *p = malloc (sizeof (int) * 100);
```

virtual address

p = 0x8000;

```
pid = fork ();
if (pid != 0) *p = 23;
```




malloc
system call
sbrk (size)
user mode
Kernel
sbrk
check if address space has space/addresses for requested size
if yes, choose a va_range, mark as used
return start of va_range
update/build va-range to PA address mappings in the page table.
set the valid & present bits to 1 in the corresponding PTE