S. Ramesh

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EDUCATION

- **Ph.D.** (Computer Science), March 1987, Indian Institute of Technology, Bombay, India.
- **B.E.**(Electronics and Communication Engineering), June 1981, Indian Institute of Science, Bangalore, India.
- **B.Sc** (Applied Sciences), May 1978, Madurai Kamaraj University, Madurai, India.

RESEARCH INTERESTS

- Formal Specification and Verification distributed and embedded Software
- Component-oriented approach to System Development
- High Level Languages, Models and Tools for Embedded Systems
- Modeling and Verification of System-on-Chip designs
- Testing Hardware and Software systems

POSITIONS HELD

- **Head**. The Centre for Formal Design and Verification of Software, Indian Institute of Technology, Bombay, India, From April 1999 till date
- **Professor**. Indian Institute of Technology, Bombay, India. From October 1998 till date
- **Visiting Professor**. Texas Instruments India R&D Centre, Bangalore, Sept. - Dec. 2003.
- **Visiting Professor**. National Information and Communication Technology Australia, May - August 2003.
- **Visiting Professor**. School of Computer Science and Engineering, University of New South wales, Sydney, Australia, During June - July 1998, 1999, 2001 and September - October 2000.
- **Visiting Research Fellow**. GMD, Sankt Augustin, Germany, September - December 1996.
- **Associate Professor**. Indian Institute of Technology, Bombay, India. August 1994 - October 1998.

- **Assistant Professor**. Indian Institute of Technology, Bombay, India. October 1989 - July 1994.
- **Visiting Fellow**. Tata Institute of Fundamental Research, Bombay, India. January 1989 - September 1989.
- **Research Fellow**. Technische Universiteit Eindhoven,The Netherlands August 1987 - December 1988.
- **Lecturer**. Indian Institute of Technology, Bombay, India. October 1986 - July 1987.
- **Research Assistant**. Indian Institute of Technology, Bombay, India, Aug. 1986 - Sept. 1986.

Ph.D. THESES SUPERVISED

1. Ambar Ghadkari, High Level Scenerio-based Specification of Hardware and embedded software Systems (In progress).
2. Mangala Gowri Nanda, Slicing Concurrent Java Programs: Issues and Solutions, November 2001.
3. Sridhar Iyer, Efficient Reachability Analysis for Concurrent Object-oriented Programs, April 1998.
4. A. Sowmya, Autonomous Robot Motion in Complex Environments: Specification and Verification, Sept. 1991 (jointly with Prof. J.R. Issac).

MASTER'S THESES SUPERVISED

Around 30 theses in different areas of research interests given above.

HONOURS THESES SUPERVISED

Around 50 Honours theses in different areas given above.

EDITED PROCEEDINGS/BOOKS

1. Proc. of the 17th FST-TCS, LNCS Vol. 1346, Springer Verlag, Dec. 1997 (jointly with G. Sivakumar)
2. Real-Time Programming: Semantics and Verification, World Scientific Press. (under preparation, jointly with R.K. Shyamasundar)

JOURNAL PAPERS/BOOK CHAPTERS

1. Synchronous Protocol Automata for Modelling and Verification of SoC Communication Architectures, to appear in IEE Proc. Computers & Digital Techniques, 2004 (with V.J. D'Silva and A. Sowmya)
2. Tabled logic programming-based IP matching tool using forced simulation, to appear in IEE Proceedings Computers & Digital Techniques, 2004 (with P.S. Roop and A. Sowmya)
3. Assertion Checking Environment(ACE) for Formal Verification of C Programs, Journal on Reliability Engineering and System Sciences, Vol. 81, No. 3, 2003. (with B. Sharma and S.D. Dhodapkar)
4. Slicing Synchronous Reactive Programs, Electronic Notes on Theoretical Computer Science, Vol. 65, No. 1, 2002, Elsevier Press. (with G. Vinod)
5. Forced Simulation: A Technique for Automating Component Reuse in Embedded Systems, ACM Trans. on Design Automation of Electronic Systems, Vol.6 No. 4, October 2001. (with Partha S. Roop and A. Sowmya)

6. Apportioning: A Technique for Efficient Reachability Analysis of Concurrent Object Oriented Programs, IEEE Trans. on Software Engineering, Vol. 27, No. 11, 2001. (with Sridhar Iyer)

7. Languages for Asynchronoy and Synchrony, Int. Journal of Foundations of Computer Science, June 2000 (with R.K. Shyamasundar)

8. Implementation of Communicating Reactive Processes, Parallel Computing, Vol. 25, No. 6, 1999.

9. Extending Statecharts with Temporal Logic, IEEE Transaction on Software Engineering, Vol. 24, No. 3, March 1998. (with A. Sowmya)

10. Impossibility of synchronization in the presence of preemption, Vol. 8, No. 1, Journal of Parallel Processing Letters, 1998. (with C.M. Shetty)

11. Validation and Analysis of the future bus arbitration protocol: A case study, SADHANA, Academy Proceedings in Engineering Sciences, Indian Academy of Sciences, Vol. 21, Part 2, April 1996. (with F. Boussinot, R.K. Shyamasundar and R. de Sim one)

12. A direct Characterization of Completion, Journal of Theoretical Computer Scince A, Vol. 154, February 1996. (with Srinivas B.N.)

13. A Compositional Axiomatization of Statecharts, Journal of Theoretical Computer Science, Vol. 101, No. 2, July 1992. (with Hooman,J.and de Roever, W.P.)

14. Modeling Real-time Systems: Issues and Challenges, SADHANA, Academy Proceedings in Engineering Sciences, Indian Academy of Sciences, Vol. 17, Part 1, March 1992. (with Shyamasundar, R.K.)

15. On the completeness of modular Proof systems, Information Processing Letters 36, Nov. 1990.

16. A Methodology for Developing Distributed Programs, IEEE Trans. on Software Engineering, Vol.SE13,No.8, 1987. (with Mehndiratta,S.L.)

17. The Liveness Property of on-the-fly Garbage Collector: A Proof, Information Processing Letters,Nov. 1983. (with Mehndiratta,S.L.)

REFEREED CONFERENCE PUBLICATIONS

1. Automated Synthesis of Assertion Monitors Using Visual Specification, Proc. of IEEE/ACM Conference on Design Automation Test Europe, DATE 2005, IEEE Press, Feb. 2005 (with A. Gadkari).

2. A Toolset for Modeling and Verification of GALS Systems. Proc. of Computer Aided Verification, CAV 2004, LNCS, July 2004 (with S. Sonalkar, V. D'silva, N. Chandra and B. Vijayalakshmi)

3. Slicing Tools for Synchronous Reactive Programs, Proc. of the ACM SIGSFOT Int. Symposium on Software Testing and Analysis, ISSTA 2004, July 2004 (with A. Kulkarni and V. Kamat).

4. CESC: A Visual Formalism for Specification and Verification of SoCsi, Proc. of the ACM Symposium GLSVLSI 2004, April 2004. (with A. Gadkari and R. Parekhji).

5. Test Derivation for Distributed Component-based Systems, Proc. of ACM Symposium on Applied Computing, SAC'04, March 2004. (with P.Kerhalkar and A. Srinivas).

6. Synchronous Protocol Automata for Modelling and Verification of System-on-Chip Bus Architectures, Proc. of IEEE/ACM International Conference on DATE, IEEE Press, February 2004. (with V.J. D'Silva and A. Sowmya).

7. Bridge over Troubled Wrappers: Automatic Interface Synthesis, Proc. of IEEE International Conference on VLSI Design, IEEE Press, 2004. (with V.J. D'Silva and A. Sowmya).

8. Static Slicing of Reactive Programs, Proc. of IEEE International Conference on Source Code Analysis and Manipulation SCAM 2003, IEEE Press, 2003. (with A.R. Kulkarni)

9. Visual Modeling and Verification of Distributed Reactive Systems, to appear in Proc. of SAFECOMP 2003, Springer, Septemeber 2003. (with A. Iqbal, S.D. Dhodapkar, A. Battacharjee)

10. Pointer Analysis of Multithreaded Java Programs, Proc. of ACM symp. on Applied Computing - SAC'03, ACM Press, March 2003. (with M.G. Nanda)

11. k-time Forced Simulation: A Formal Verification Technique for IP Reuse, Proc. of ICCD, IEEE Press, Sept. 2002. (with Partha S. Roop and A. Sowmya).

12. Assertion Checking Environment(ACE) for Formal Verification of C Programs, Proc. of SAFECOMP 2002, LNCS Vol. 2434, Springer, September 2002. (with Babita Sharma and S.D. Dhodapkar)

13. A Formal Approach to Component Based Development of Synchronous Programs, Proc. of ASP-DAC 2001, IEEE Press, February 2001. (with P. Roop and A. Sowmya)

14. Refinement and Efficient Verification of Synchronous Programs, IFAC Workshop on Distributed Computer Control Systems, Pergamon Press, December 2000.

15. Slicing Concurrent Programs, Proc. ACM SIGSOFT International Conference on Software Testing and Analysis (ISSTA 2000), ACM Press, August 2000 (with M. Gowri Nanda)

16. Automated component adaptation by forced simulation, Proc 5th Australasian Computer Architecture Conference, ACAC 2000, Canberra, Feb 2000, ed. G. Heiser, Australian Computer Science Communications, Vol 22, No 4, p. 74-81, IEEE Computer Sci Society, Los Alamitos, Cal. (with P. Roop and A. Sowmya)

17. Automatic Component Matching using Forced Simulation, Proc. of 13th Int. Conf. on VLSI Design, IEEE Press, January 2000. (with P. Roop and A. Sowmya)

18. Validation of Pipelined Processor Designs using Esterel Tools: A Case Study, Proc. of CAV '99, LNCS Vol. 1633, 1999. (with P. Bhaduri)

19. Efficient Translation of Statecharts into Hardware Circuits, Proc. of 12th Int. Conf. on VLSI Design, IEEE Press, January 1999.

20. Apportioning: A Technique for Efficient Reachability Analysis of Concurrent Object-oriented Programs, Proc. of 5th Int. Conf. on High Performance Computing, IEEE Press, December 1998. (with Sridhar Iyer)

21. Communicating Reactive State Machines: Design, Model and Implementation, IFAC Workshop on Distributed Computer Control Systems, Pergamon Press, September 1998.

22. Formal specification and verification of hardware designs, Proc. of SPIE, Vol. 3412, Photomask and X-Ray Mask Technology V, Kawasaki, Japan, 1998. (with S. S. S. P. Rao, G. Sivakumar and P. Bhaduri)

23. A Tool-Suite for Reachability Analysis of Concurrent Object-Oriented Programs, Proc. of Joint APSEC '97 and ICSC'97, IEEE Press, December 1997. (with Sridhar Iyer)

24. Concurrent Logic Programming and pi calculus, Fourteenth International Conference on Logic Programming, ICLP '97 (poster presentation), July 1997. (with S. Mahajan)

25. A semantics-preserving transformation of statecharts to FNLOG, 20th IFAC/IFIP Intl Workshop on Real-time Programming, Fort Lauderdale, Florida, USA, Nov 6-10 1995. (with A. Sowmya)

26. Control design for Autolab using the reactive paradigm, 13th IFAC Intl Workshop on Distributed Computer Control Systems, Toulouse-Blagnac, France, Sept 27-29, Elsevier Science Ltd. 1995. (with S. Bajaj, A. Sowmya, and N. Ahmed)

27. Verification of CRP programs, Proc.of Conference on Hybrid Systems and Autonomous Control, LNCS, Springer 1994. (with Shyamasundar, R.K.)

28. Languages for Asynchrony and Synchrony, Proc. of Fault-Tolerant and Real-time Symposioum, LNCS, Springer, 1994. (with Shyamasundar, R.K.)

29. Communicating Reactive Processes, Proc. of 20th Annual ACM SIGPLAN-SIGACT Symposium on POPL, January, 1993 (with Berry,G., and Shyamasundar, R.K.)

30. Fully Abstract Semantics for Higher Order Communicating Systems, Proc. of Mathematical Foundations of Computer Science, LNCS Vol. 629, Springer Verlag, Berlin, 1992.

31. Verification of Timing Properties in a Statecharts-based Model of Real-time Reactive Systems, In Distributed Computer Control Systems, IFAC Workshop series 1992 (H. Kopetz and M.G. Rodd, Eds.), Vol. 3, Pergamon Press, Oxford. (with A. Sowmya)

32. A statechart approach to specification and verification of autonomous mobile robot behavior, Proc. Int. Conf. Automation, Robotics and Computer Vision - ICARCV '90, Singapore, Sept. 1990. (with A. Sowmya, and Issac, J.R.)

33. A real-time reactive model of an AMR, Proc. Int. Conf. on CONTROL '90, Lugano, 1990. (with A. Sowmya, and Issac, J.R.)

34. A Compositional Axiomatization of Safety and Liveness properties of Statecharts, Proc. of Int. BCS-FACS Workshop on Semantics for Concurrency, Leicester, July 1990. (with Hooman, J., and de Roever, W.P.)

35. A Compositional Semantics of Statecharts, Proc. of Formal Models of Concurrency, Novosibersk, Oct. 1989. Also in J.W. de Bakker, 25 Jaar Semantiek, Liber Amicorum, CWI, April 89. (with Hooman, J., and de Roever, W.P.)

36. A New Efficient Implementation of CSP with output guards, Proc. of 7th Int. Conf. on Distributed Computing Systems, IEEE, Berlin, Aug.1987

37. A New and Efficient Implementation of Multiprocess Synchronization Mechanisms, Proc. of PARLE Conf. Vol. 2,LNCS 259,Springer Verlag, Eindhoven, 1987

38. A New Class of High Level Programs for Distributed Computing Systems, Proc. of the 5th Conf. on FSTTCS, LNCS 206, Springer Verlag, Berlin,Dec.1985. (with Mehndiratta,S.L.)

39. Developing distributed Implementations of Abstract Data Types, Proc. of ICS Conf.,Taiwan,Dec.1983. (with Mehndiratta,S.L.)

RESEARCH GRANTS AND CONTRACTS

1. 'Centre for Formal Design and Verification of Software',
   Co-investigators: Prof. G. Sivakumar and Prof. S. Chakraborty,
   Sponsor: BRNS, Duration: 1999-2004, Budget: Rs. 3.06 Crores

2. Testing and Conformance Checking in Object-oriented systems,
   Sponsor: TCS, Pune, Fund: Rs. 3 lakhs, Duration: 2001 - 2003

3. 'State-based Specification and Logic Programming-based Verification of Embedded Systems'
   PI: Prof. A. Sowmya, UNSW, Australia, CI: Prof. I.V. Ramakrishnan, SUNY Stony Brooke, USA
   Sponsor: Australian Research Council - IREX Scheme, Duration: 2001 - 02

4. 'Programming Dynamical Real Time systems',
   Sponsor: U.S. Army Research Laboratory and US-IF,
   Co-investigators: Prof. R.K. Shyamasundar, TIFR, Mumbai and Prof. Krithi Ramamrithm, U. Mass., USA,
   Duration: 1998-2000, Budget: Rs. 13 lakhs.

5. 'New methodologies and tool-support for computer communication protocol testing',
   Sponsor: AICTE (under R&D project), Other Investigators: Prof. S.L. Mehndiratta ,
   Duration: 1996 - 99. Budget: Rs. 7 lakhs.

6. 'Efficient verification of synchronous programs'
   Sponsor: TIL, Mumbai, Duration: 1996 - 97

7. 'Formal specification and development of real-time reactive programs',
   Sponsors: Indo-French Centre, New Delhi.
   Other Investigators: Prof. RK. Shyamasundar, TIFR, Bombay and Prof. G. Berry, INRIA, Sophia Antipolis, France.
   Duration: 1992-95, Budget: Rs. 12 lakhs.

8. 'Simulation of Petri Nets',
   Sponsor: Tandem Computers Ltd., Duration: 1993 - 94, Budget: Rs. 1.2 Lakhs.

INDUSTRIAL CONSULTANCY PROJECTS

1. Feasibility Study of Formal Verification of On board Software, VSSC, Trivandrum, Other investigators: Prof. S. Chakraborty, Mr. S.D. Dhodapkar, Budget: Rs. 2.3 Lakhs, Feb. - June 2003.

2. Testing of FPGAs: VSSC, Trivandrum, Other investigators: Prof. S.S.S.P. Rao, Fund: Rs. 7 lakhs, 2001 - 03.

3. Testing of i960 micro processor, Sponsor: VSSC, Trivandrum, Other investigators: Profs. S.S.S.P. Rao and G. Sivakumar, Budget: Rs. 8 Lakhs, 2000 - 01.

4. Formal Verification of Get-U-Home Panel Software,
   Sponsor: ADA, Bangalore, Budget: Rs. 4,94,500, 2001 - 02 Jointly with S. Chakraborty IIT Bombay, S.D. Dhodapkar, BARC, Mumbai.

5. Model Checking on Industrial designs, Sponsor: Texas Instruments, Bangalore,
   Budget: Rs. 75,000, 2001 - 02 Jointly with S. Chakraborty

6. A Semantic Basis for DDMP, Sponsor: SAS, Bangalore, Budget; Rs. 75,000, 1999 - 2000.

RESEARCH COLLABORATION

1. Professor W. P. de Roever, Institut fur Informatik und Praktische Mathematik, Christian- Albrechts Universitat, Kiel, Germany

2. Professor G. Berry, INRIA, Sophia Antipolis, France

3. Professor R.K. Shyamasundar, Tata Institute of Fundamental Research, Mumbai.

4. Dr. J. Hooman, Computing Science department, Katholique Universite Nijmegan, The Netherlands.

5. Dr. A. Sowmya, School of Computer Science and Engineering, University of New South wales, Australia.

6. Professor A. Poigne, GMD Sank Augustin, Germany

7. Professor D. Bjorner, Technical University of Denmark, Lyngby, Denmark
8. Dr. P. S. Roop, Dept. of Electrical and Electronic Engineering, University of Auckland, New Zealand.
9. Dr. R. Parekhji, Texas Instruments, Bangalore.

PROFESSIONAL ACTIVITIES

1. Serving as an Indian Member of the IFAC Technical Committee CCD (Distributed Computer Control).
2. Served as co-chair for the Seventeenth annual Conference on Foundations of Software Technology and Theoretical Computer Science.
3. Served on the Program Committee of several international and national conferences that include
   - International Confernece on VLSI Design and Embedded Systems, 2002 - 2004.
   - Asia South Pacific Design Automation Conferences 2001-2002,
   - Formal Techniques in Real-Time and Fault-Tolerant Systems (FTRTFT 2000),
   - IFAC conference on Distributed Control Systems 2000,
   - First Asian Computer Science Conference 1995,
   - Foundations of Software Technology and Theoretical Computer Science,
4. Refereed a number of papers for the international journals on Parallel Processing, Distributed Computing and Real-Time Systems, Software Practice & Experience.
5. Served as expert member in national and international accreditation committees and selection boards.

TALKS AND COLLOQUIA (select ones)

- Series of talks on Modeling and Verification of SoC designs and Embedded Software at University of NewSouthwales, Sydney, May - Aug. 2003.
- Series of talks on Modeling and Verification of Embedded Systems at University of NewSouthwales, Sydney, May - Aug. 2003.
- Invited talks at Univ. of Reading and Univ. of Southampton during April 2002.
- Invited talk at the workshop on Real-Time Systems held in University of New South Wales, Australia, in July 1998.
- Key-note address at ISRO workshop on Software Engineering, IWSE-94, Trivandrum, held during July 1994.
- National Workshop on Software Reliability Engineering, WSRE-92, at BARC, Bombay,
- Indo-US workshop on Co-operative Research Programme, Bangalore, Aug. 1992,
- the meeting of the IFIP working group on Programming Languages, held at TIFR, Bombay, 1992,
- Dept. of Computer Science, Aalborg University, Aalborg, Denmark, Jan. 1992 ,
- Dept. of Computer Science, Technical University of Denmark, Lyngby, 1992.
- the workshop on Logics and Models of Concurrent Programs, Bangalore, July, 1989,

- Biweekly seminar at LITP, Paris, 1988.

OTHER PROFESSIONAL ACTIVITIES

1. Gave half-a-day tutorial on Formal verification as part of the International Conference on Information Technology, Bhubaneshwar, December 2002.
2. Organized a four-day workshop on Formal Verification for Safety-critical Industrial Systems held during December 2002.
3. Gave part of a tutorial titled "Functional Verification of System-on-Chip Designs" at the 7th Asia Pacific Design Automation Conference nd the 15th International Conference on VLSI Design held in Bangalore during Jan. 2002.
4. Prepared course material for the Course 'Parallel Processing'.
   This is part of Project IMPACT, sponsored by the World Bank. A number of other members were also involved in this project.
5. Prepared Course material for the Course 'Symbolic Logic and Logic Programming'.
   This is part of Project IMPACT, sponsored by the World Bank. The other members involved in this project were: Dr. G. Venkatesh and Dr. G. Sivakumar, IIT Bombay.
6. Conducted a day-long lecture on 'Finite State Machines and Propositional Logic' as part of a course to Messers TCS, during March - April 2000.
7. Conducted a day-long lecture on 'Program Testing' as part of a course to Messers. Origin, during March - April 2000.
8. Conducted a day-long lecture on 'Program Testing' as part of a course to Messers Origin, during May - June 1999.
9. conducted a two-day course titled 'Finite State Machines' for TCS Mumbai, jointly with Dr. A. Sanyal.
10. Conducted a course titled 'Principles of programming languages' for working professionals, jointly with Dr. G. Venkatesh and Dr. A. Sanyal, December 1994 - January 1995