

GCC Internals: A Conceptual View – Part II

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PART I

- GCC: Conceptual Structure
- C Program through GCC
- Building GCC

PART II

- Gimple
- The MD-RTL and IR-RTL Languages in GCC
- GCC Machine Descriptions

Part I

Gimple

The Goals of GIMPLE are

- Lower control flow
Program = sequenced statements + unrestricted jump
- Simplify expressions, introduce temporary variables as needed
Typically: two operand assignments!
- Simplify scope
move local scope to block begin – including temporaries

Notice

Lowered control flow → nearer to register machines + Easier SSA!

Tree manipulation passes (`tree-optimize.c`)

- **Gimplifier** case analyzes GENERIC nodes, calls corresponding gimplifier.
 $\{\text{Gimple}\} = \{\text{AST/Generic}\} - \{\text{Control flow nodes}\}$
- **Node type** specific gimplifiers
- **Optimization passes** on tree representation, and
- **Translate** to next IR, i.e. RTL
 - Depth first traverse the “input” Gimple representation
 - Generate a linear list RTL representation

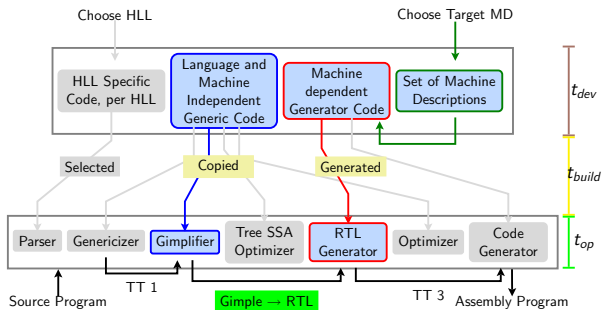
BUT WE HAVE A PROBLEM . . .

Gimple → RTL Translation Table – Part I

PROBLEM: Gimple (m/c indep.) → RTL (m/c specific)!

TO DO : Implement m/c indep. to m/c dep. translation at t_{dev}

GIVEN : the actual target will be known only at t_{build}

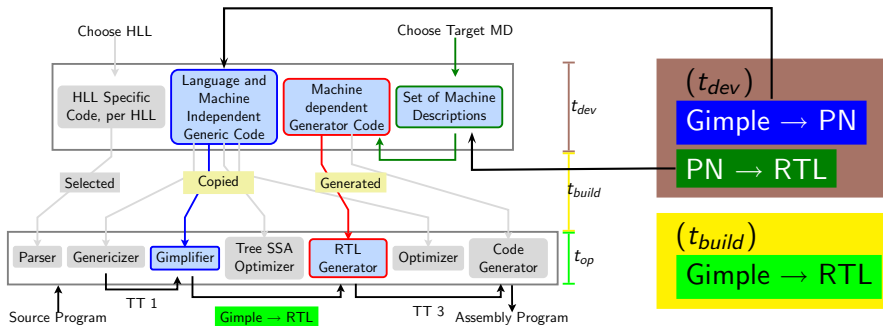


Gimble \rightarrow RTL Translation Table – Part I

PROBLEM: Gimble (m/c indep.) \rightarrow RTL (m/c specific)!

TO DO: Implement m/c indep. to m/c dep. translation at t_{dev}

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`MODIFY_EXPR``(set (<dest>) (<src>))`



MODIFY_EXPR

"movsi"

(set (<dest>) (<src>))

Standard Pattern Name

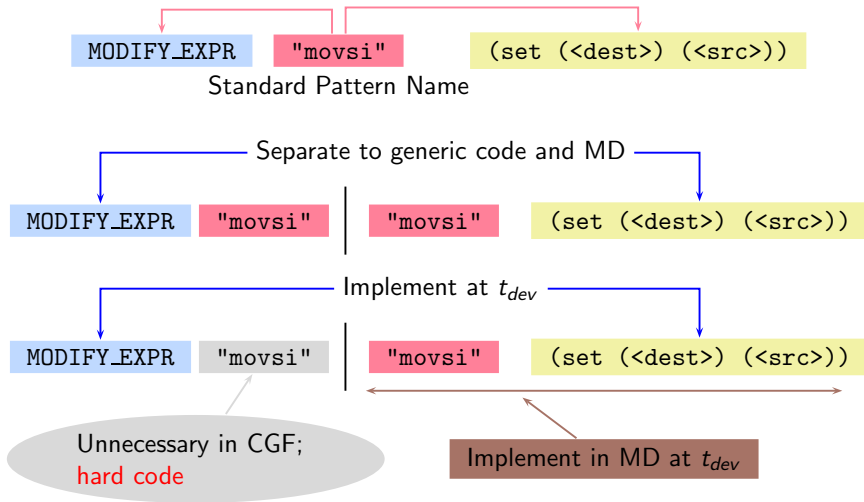
Separate to generic code and MD

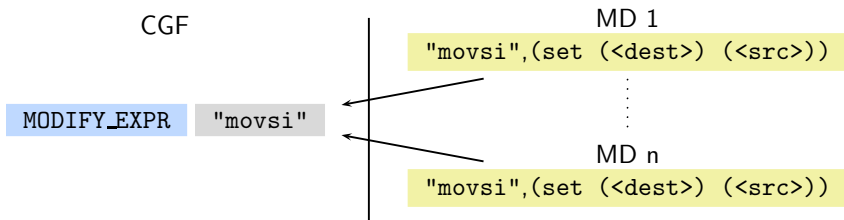
MODIFY_EXPR

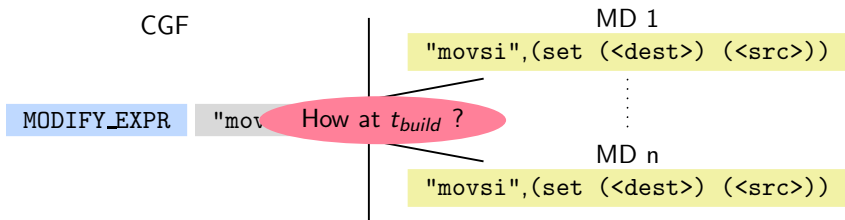
"movsi"

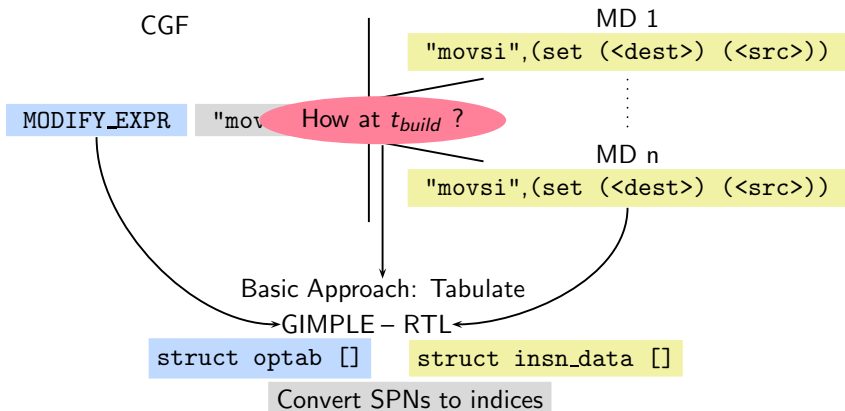
"movsi"

(set (<dest>) (<src>))









Part II

The MD-RTL and IR-RTL Languages in GCC

Goal 1: Specify target instruction semantics at t_{dev}

Capture target instruction semantics as RTXs

Use MD constructs and operators → The MD-RTL Language

Goal 2: Represent input program at t_{op}

- Lower data
- “Express” the “captured” target semantics in IR
- Goal: Every RTX of last RTL pass = unique ASM string.

Use IR constructs and operators → The IR-RTL Language

Notice

Lowered data and procedures → nearer to typical hardware

Goal 1 Example: Specifying target inst. semantics

```
(define_insn
  "movsi"
  (set
    (match_operand 0 "register_operand" "r")
    (match_operand 1 "const_int_operand" "k")
  )
  "" /* C boolean expression, if required */
  "mov %0, %1"
)
```

Goal 1 Example: Specifying target inst. semantics

Define new inst. pattern

(Standard) Pattern Name

```
(define_insn
  "movsi"
  (set
    (match_operand 0 "register_operand" "r")
    (match_operand 1 "const_int_operand" "k")
  )
  "" /* C boolean expression, if required */
  "mov %0, %1")
```

RTX: Capture semantics
of target inst.

target asm inst. =
Concrete syntax for RTX

Goal 1 Example: Specifying target inst. semantics

MD RTX

MD constructs

```
(define_insn  
  "movsi"  
  (set  
    (match_operand 0 "register_operand" "r")  
    (match_operand 1 "const_int_operand" "k")  
  )  
  "" /* C boolean expression, if required */  
  "mov %0, %1"  
)
```

Operators

RTL Expression (RTL)

From Goal 1 to Goal 2: RTL at t_{build}

Alert: At t_{build}

Convert MD-RTL at $t_{develop}$ to RTL data structures, and compile.

The Data Structure for RTL Objects (In `rtl.h`)

```
struct rtx_def { /* RTL codes (e.g. SET) enum-med
    from $GCCHOME/gcc/rtl.def */
    ENUM_BITFIELD(rtx_code)      code : 16;
    ENUM_BITFIELD(machine_mode) mode : 8;
    unsigned int                 jump : 1;
    /* ... a few such flags */
    union u {
        rtxunion      fld[1];
        HOST_WIDE_INT hwint[1];
    };
};
```

Goal 1 to Goal 2: Gimple → RTL Translation Table

Conversion of RTL from Textual to Internal Form

```
(define_insn
```

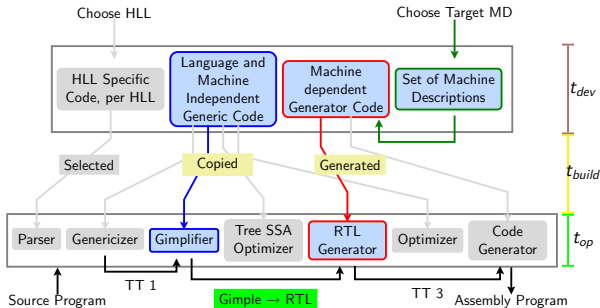
```
  "movsi"
```

```
  (set (op0) (op1))
```

```
  ""
```

```
  "mov %0, %1")
```

t_{dev}



Goal 1 to Goal 2: Gimple → RTL Translation Table

Conversion of RTL from Textual to Internal Form

```
(define_insn  
  "movsi"  
  (set (op0) (op1))  
  ""  
  "mov %0, %1")
```

t_{dev}

```
rtx  
gen_movsi (rtx operand0, rtx operand1)  
{  
  ...  
  emit_insn (gen_rtx_SET (VOIDmode, op0, op1));  
  ...  
}
```

t_{build}

Goal 1 to Goal 2: Gimple → RTL Translation Table

Conversion of RTL from Textual to Internal Form

```
(define_insn  
  "movsi"  
  (set (op0) (op1))  
  ""  
  "mov %0, %1")
```

t_{dev}

```
rtx  
gen_movsi (rtx operand0, rtx operand1)  
{  
  ...  
  emit_insn (gen_rtx_SET (VOIDmode, op0, op1));  
  ...  
}
```

t_{build}

Goal 1 to Goal 2: Gimple \rightarrow RTL Translation Table

Conversion of RTL from Textual to Internal Form

```
(define_insn  
  "movsi"  
  (set (op0) (op1))  
  ""  
  "mov %0, %1")
```

t_{dev}

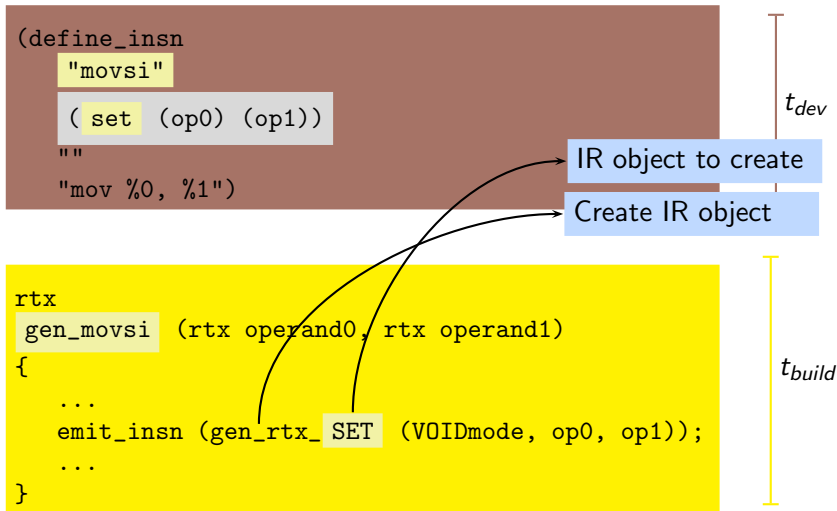
IR object to create

```
rtx  
gen_movsi (rtx operand0, rtx operand1)  
{  
  ...  
  emit_insn (gen_rtx_SET (VOIDmode, op0, op1));  
  ...  
}
```

t_{build}

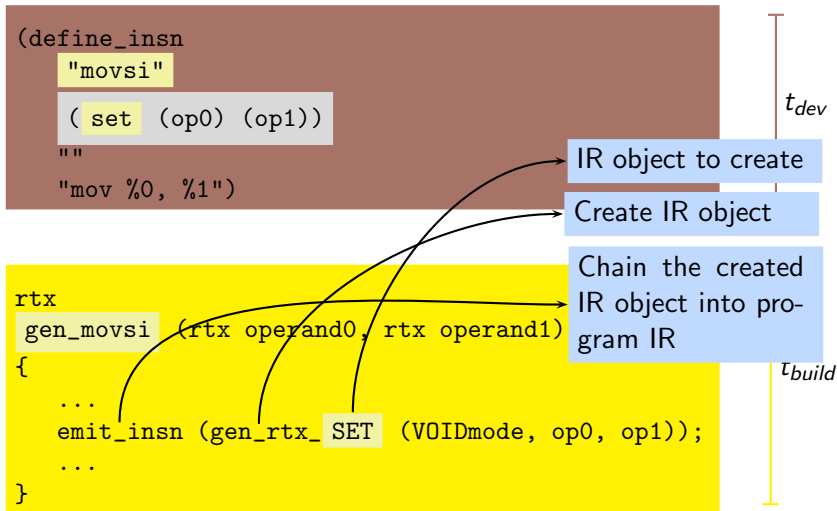
Goal 1 to Goal 2: Gimple \rightarrow RTL Translation Table

Conversion of RTL from Textual to Internal Form



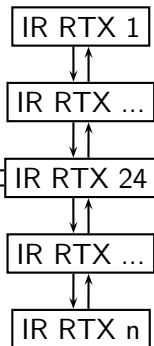
Goal 1 to Goal 2: Gimple \rightarrow RTL Translation Table

Conversion of RTL from Textual to Internal Form



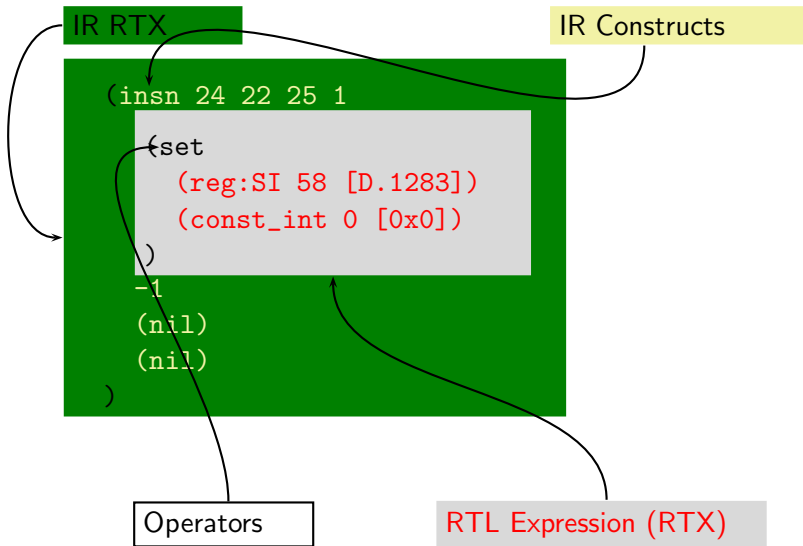
RTL at t_{op} : Example of RTL in use as IR

```
(insn 24 22 25 1
  (set
    (reg:SI 58 [D.1283])
    (const_int 0 [0x0])
  )
  -1
  (nil)
  (nil)
)
```



See: RTL dump in “C Program through GCC”

RTL at t_{op} : Example of RTL in use as IR



RTL at t_{op} : Example of RTL in use as IR

Instruction position in sequence

Previous inst.

Next inst.

```
(insn 24 22 25 1
```

```
(set  
  (reg:SI 58 [D.1283])  
  (const_int 0 [0x0])  
)
```

```
-1
```

```
(nil)
```

```
(nil)
```

```
)
```

Instantiation of RTX
specified in MD.

Register #58 matches
the corresponding
match_operand spec.

Similarly, for the
next operand.

RTL at t_{op} : Example of RTL in use as IR

```
(insn 24 22 25 1
  (set
    (reg:SI 58 [D.1283])
    (const_int 0 [0x0])
  )
  -1
  (nil)
  (nil)
)
```

Note:

RTL is incomplete.

Hard register for
pseudoregister #58
unknown (yet).

Allocate: #58 = eax

RTL is now complete.

Instantiated RTL is target dependent because the RTL
specified in MD captures target instruction semantics.

Part III

GCC Machine Descriptions

Why MD at t_{dev} ?

MDs are written in MD-RTL

Main Purpose: Gimple \rightarrow IR-RTL Translation at t_{run}

Gimple

m/c indep.

Known at t_{dev}

Single “instance”

IR-RTL

m/c specific.

Unknown at t_{dev} , known at t_{build}

Per target “instance”

Other Purposes

- IR-RTL Manipulations
 - Gimple \rightarrow IR-RTL
 - IR-RTL \rightarrow IR-RTL (combine or split)
 - IR-RTL \rightarrow Target ASM
- Support
 - Programmer support through convenience constructs
 - Additional heuristics for Instruction selection

- Processor instructions useful to GCC
- Processor characteristics useful to GCC
- Target ASM syntax
- IR-RTL \rightarrow IR-RTL transformations
(GCC code performs the transformation computations,
MD supplies their *target patterns*)
- Target Specific Optimizations

Syntactic Entities in GCC MD

Two kinds:

- Necessary Specifications

- Processor instructions useful to GCC
 - One Gimple → One IR-RTL
 - One Gimple → More than one IR-RTL
- Processor characteristics useful to GCC
- Target ASM syntax
- IR-RTL → IR-RTL transformations
- Target Specific Optimizations

`define_insn`

`define_expand`

`define_cpu_unit`

part of `define_insn`

`define_split`

`define_peephole2`

- Programming Conveniences

- `define_insn_and_split`
- `define_constants`
- `define_cond_exec`
- `define_automaton`

Tip

See: `$GCCHOME/gcc/rtl.def`.

Focus on the RTX!

- Target semantics are in the RTX!
- Target ASM syntax is one argument of `define_insn`
- The set of `define_insns` must be “complete”.
- All IR-RTL manipulations must have a `define_insn`.

Example

```
(define_insn "trap" ; "trap" pattern in i386.md
  [(trap_if (const_int 1) (const_int 5))]
  "" "int $5")
```

```
(define_insn "trap" ; "trap" pattern in mips.md
  [(trap_if (const_int 1) (const_int 0))]
  "" "break 0") ; some target asm details ignored
```