



Uday Khedker
IIT Bombay

Talk Title:
Compilation Overview

Topic:
Outline

An Overview of
Compilation Phases

Incremental
Construction of
Compilers

My Vision for SCLP

My Vision of SCLP



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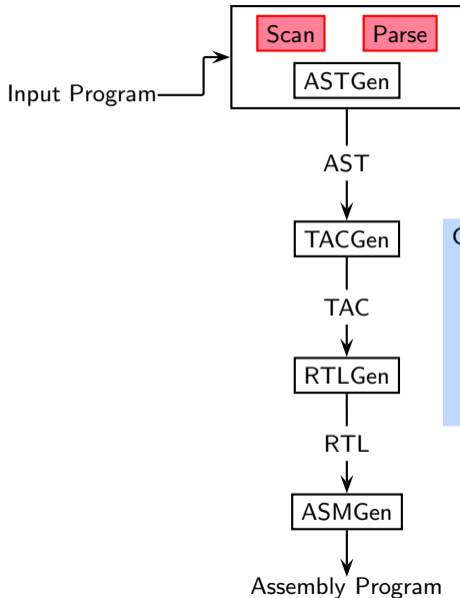
Incremental
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My Vision for SCLP

Generated from Specs

Manually written

SCLP: The Grand Plan



Conventions used in picture

- Boxed text represents a component of the language processor or an external tool
- Unboxed text shows input or output



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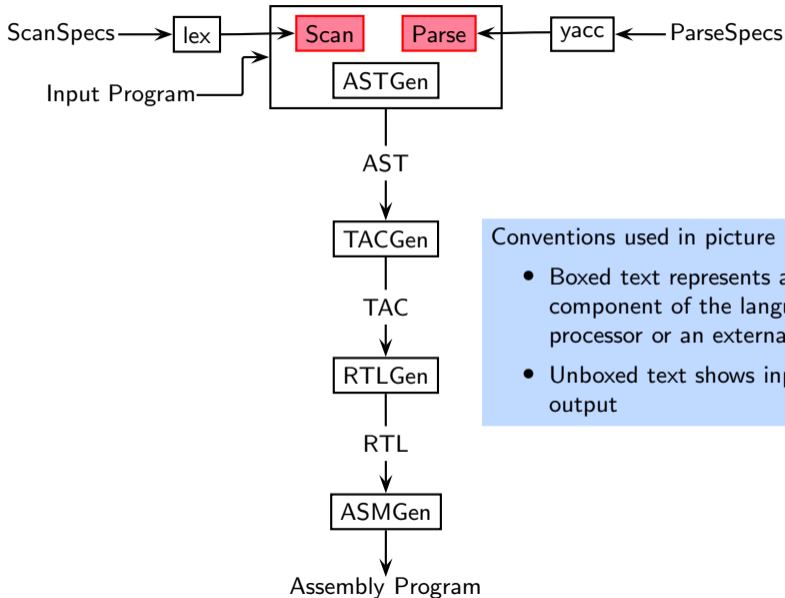
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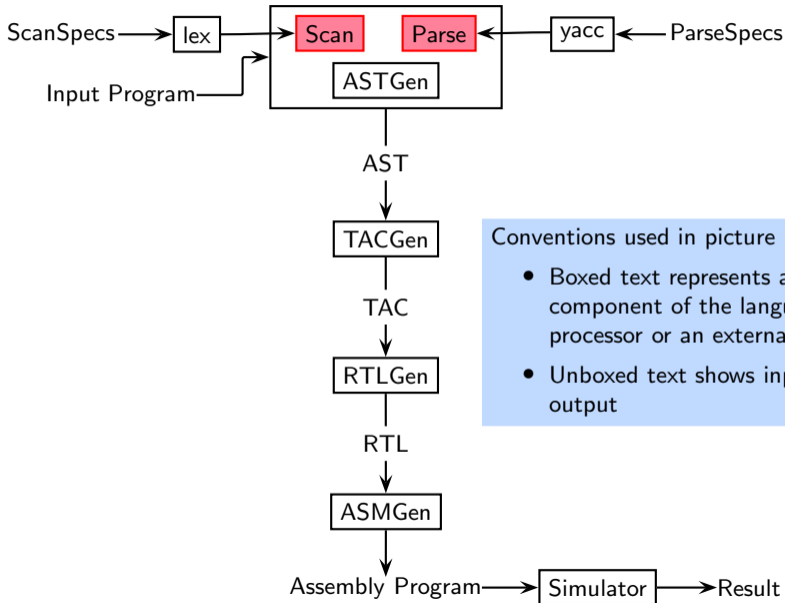
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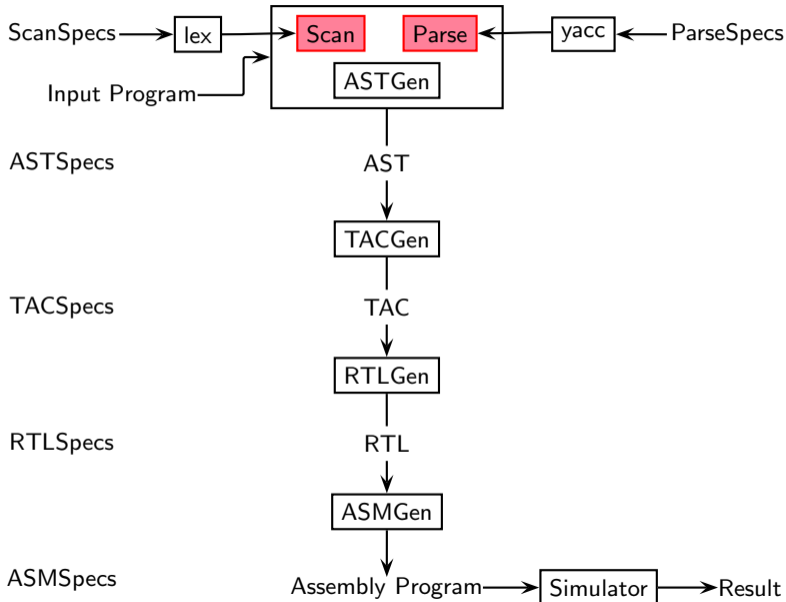
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Generated from Specs

$AST \in ASTSpecs$

TransRules

$TAC \in TACSpecs$

TransRules

$RTL \in RTLSpecs$

TransRules

$ASM \in ASMSpecs$

Manually written

AST

TACGen

TAC

RTLGen

RTL

ASMGGen

Assembly Program

Simulator

Result

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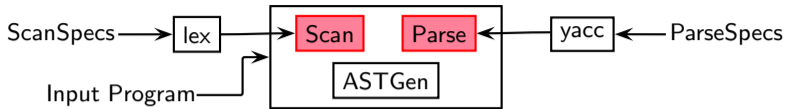
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AST \in ASTSpecs

AST

TransRules



TAC \in TACSpecs

TAC

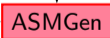
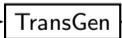
TransRules



RTL \in RTLSpecs

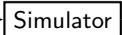
RTL

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ASM \in ASMSpecs

Assembly Program



Result

Manually written

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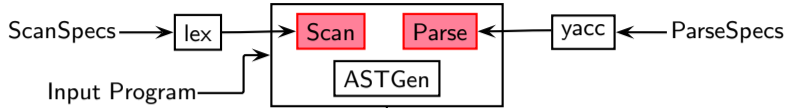
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AST \in ASTSpecs

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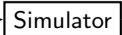
RTL \in RTLSpecs

TransRules



ASM \in ASMSpecs

Assembly Program



Result

Manually written

Pioneered by the BTP of Michelle's group by defining

- the notion of a compiler state and distinguishing it from a program state
- translation rules
- implementing a generator for rules

They developed their intuitions of "boiler plate code" by implementing ASMGGen manually for SPIM

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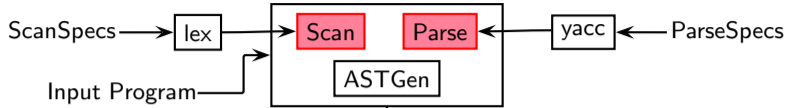
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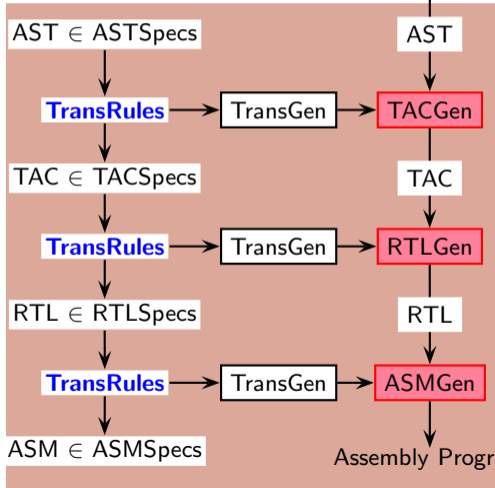
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The first idea of work is to use the concept of compiler state and

- write translation rules and associated generators for TACGen and RTLGen
- generate ASMGen for a different RISC processor using the simulator RIPES

This requires separating out spim information from the TransGen code into separate tables as specifications

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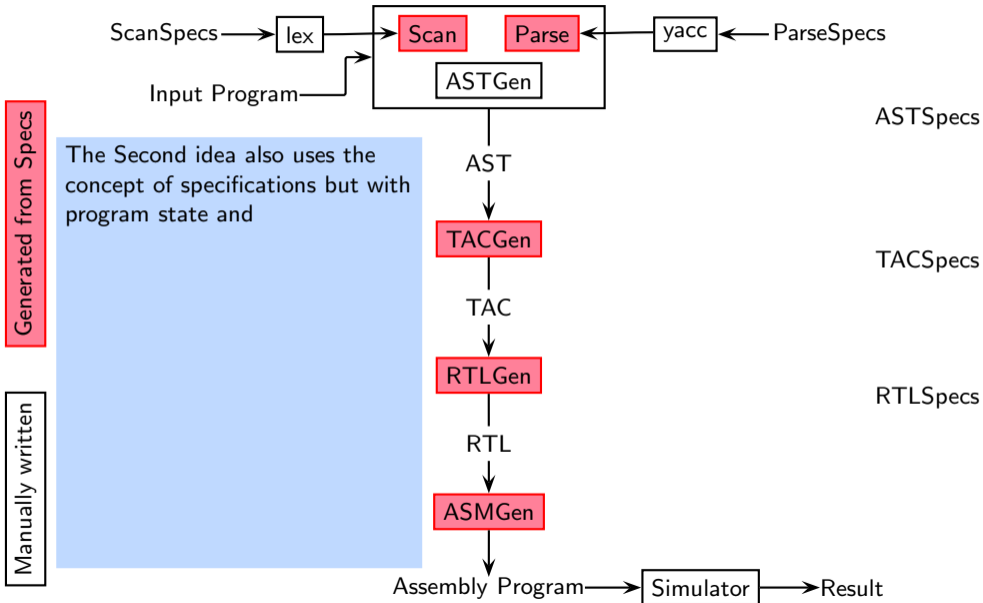
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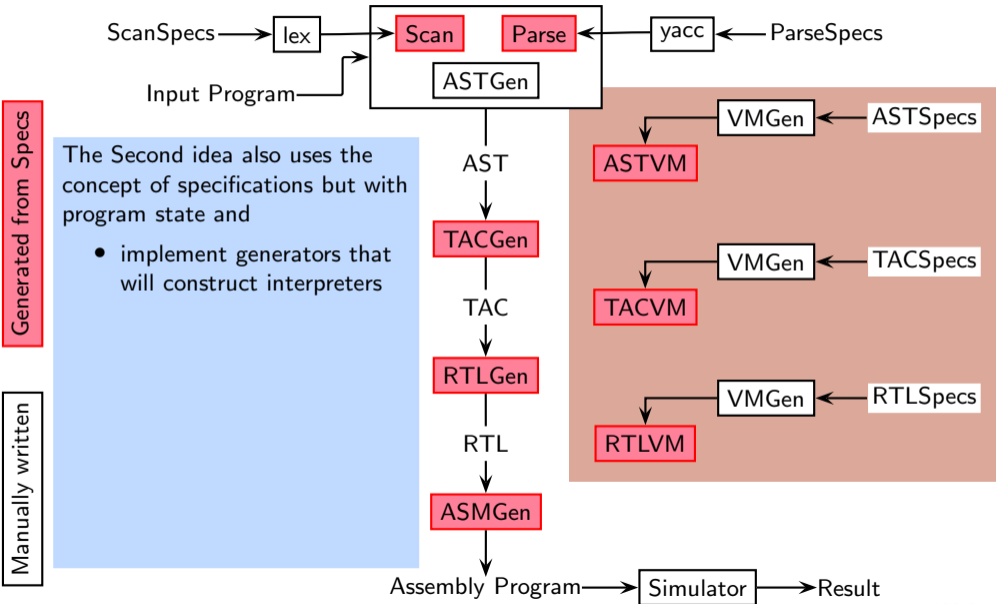
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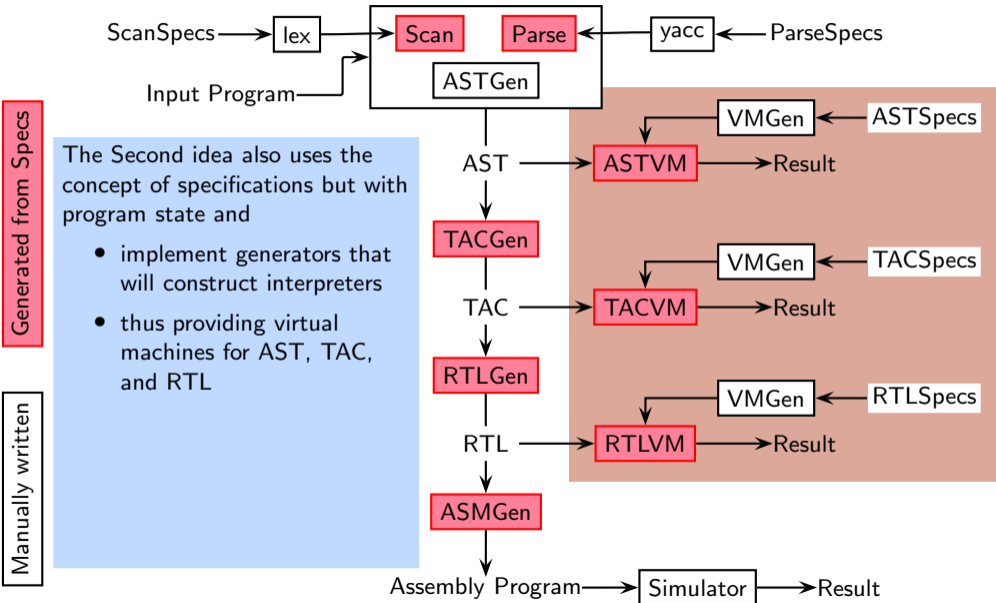
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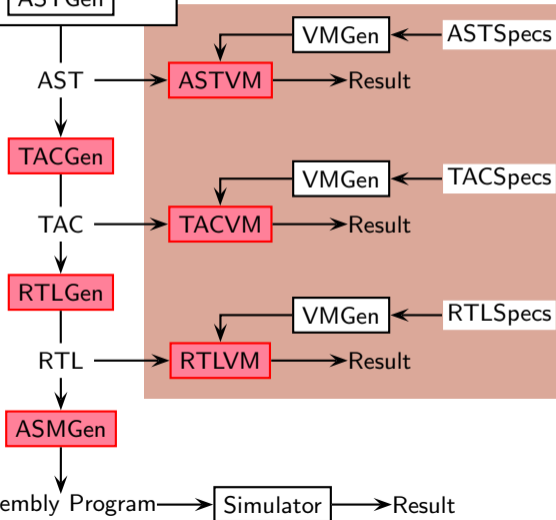
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The Second idea also uses the concept of specifications but with program state and

- implement generators that will construct interpreters
- thus providing virtual machines for AST, TAC, and RTL

Manually written

ASM interpreter is external





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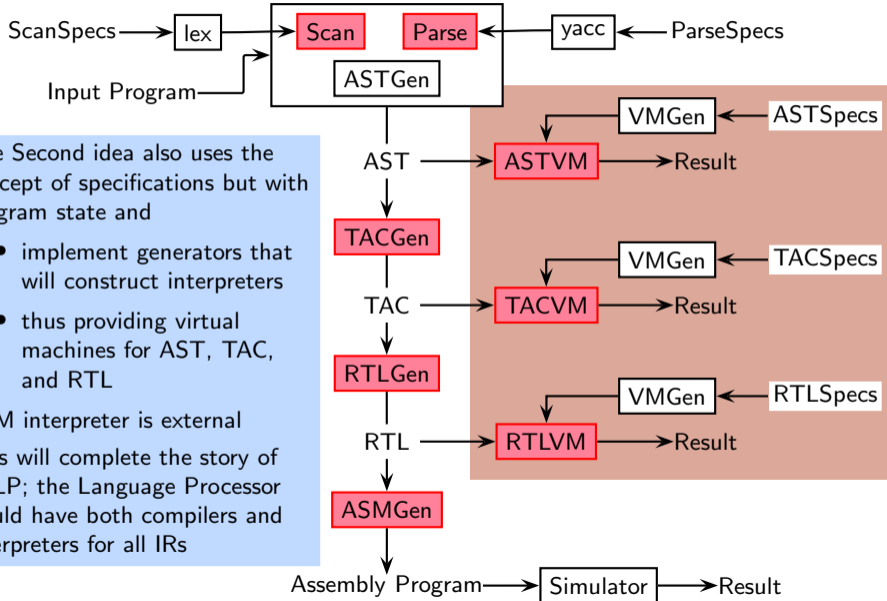
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ASM interpreter is external
This will complete the story of SCLP; the Language Processor would have both compilers and interpreters for all IRs



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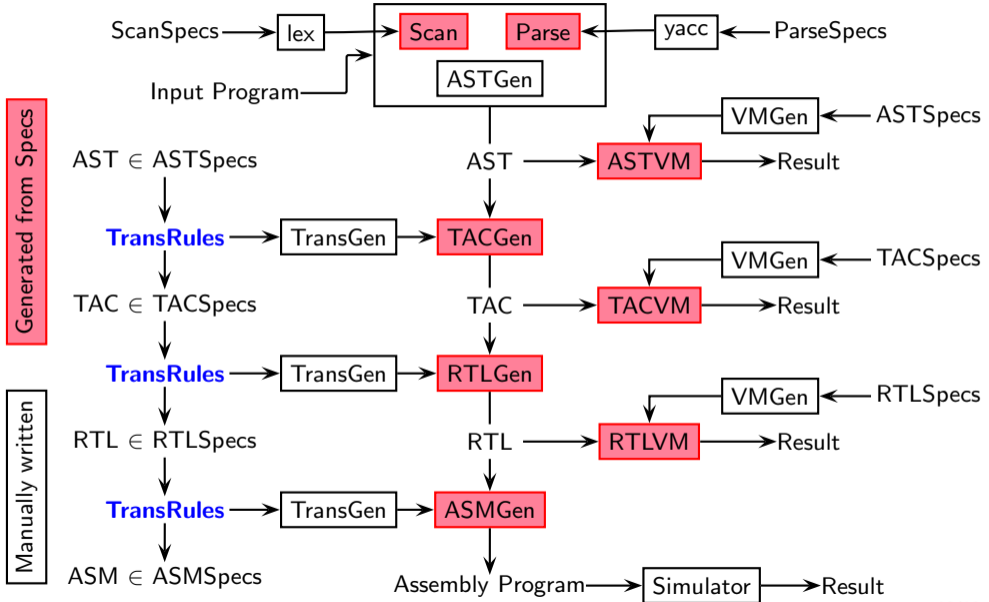
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